

# Previously Unobserved Effects of Delay on Current-Mode Control

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**Abstract**--A new sampled-data model for the current-mode controlled buck converter includes for the first time the effects of delay in the current loop. Modified z-transforms are used in this new model for constant frequency trailing-edge modulation. Realistic amounts of delay are found to be particularly significant when the buck converter is operating in the continuous conduction mode near the discontinuous conduction mode boundary. The new model is used to predict the loop gain measurements obtained with the digital modulator and with conventional measurement techniques. It is shown that conventional loop gain measurement techniques are insufficient to measure the loop gain in this region of operation. It is also shown that the digital modulator can add a significant amount of delay, thereby altering the loop gain of the circuit being measured. However, if care is taken to minimize this delay, a good loop gain measurement can be achieved. The new model accurately predicts the boundary condition for subharmonic instability. In addition, it reduces to Ridley's current-mode control model for the case of zero delay.

## I. INTRODUCTION

A new incremental, sampled-data model has been developed for the current-mode controlled buck converter [1]. With the use of modified z-transforms [2], the effects of delay are modeled. It is shown for the first time that delay present in the circuit will affect the magnitude of the current loop gain thereby causing apparent discrepancies in current loop gain measurements [3]. This is in contrast to non-switched circuits where only the phase would be altered. This alteration in the magnitude of the loop gain is most pronounced under the conditions of continuous conduction mode operation with light load, that is, near the discontinuous conduction mode boundary. It is also shown that for zero delay, this new model agrees with the model proposed by Ridley [4].

This new model is used to determine the correct method of measuring the current loop gain. It is shown that the conventional way of measuring the loop gain in non-switched circuits [5] is inadequate to measure the current loop gain of the current-mode controlled buck converter. It is also shown that the digital modulator proposed by Cho and Lee [6] can be used to measure the current loop gain, but only if certain precautions are taken. The digital modulator will introduce additional delay into the circuit being measured, and as a result the magnitude of the current loop gain will be altered. This may explain the discrepancies

discussed by Tan that exist between Ridley's model and measurements obtained with the digital modulator [3]. However, a good loop gain measurement can be obtained if the delay introduced by the digital modulator is minimized.

## II. DERIVATION

Fig. 1 shows the current-mode controlled buck converter. The type of current-mode control investigated is constant frequency with trailing edge modulation. The switching period  $T$  is constant and the clock initiates the on-time of the gating waveform  $h(t)$ .

The inductor current  $i_L(t)$  may be calculated using the voltage  $v_i(t)$  across the diode and the initial conditions of  $L$  and  $C$ . The current  $i_L(t)$  may be divided into two parts:

$$i_L(t) = I_L(t) + \hat{i}_L(t) \quad (1)$$

$I_L(t)$  represents the cyclic steady state inductor current. Steady-state refers to the case for which the duty cycle of the gating signal  $h(t)$  is a constant  $D$ . The steady-state gating signal is denoted as  $H(t)$ . The current  $\hat{i}_L(t)$  is the incremental inductor current resulting from a perturbation  $\hat{h}(t)$  in the gating waveform. Likewise, the voltage  $v_i(t)$  across the diode can be divided into a steady state and an incremental part:

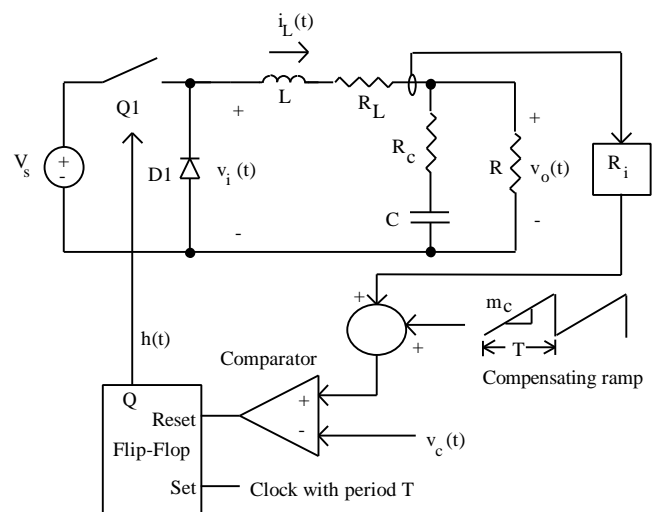


Fig. 1 Current-mode controlled buck converter.

$$v_i(t) = V_i(t) + \hat{v}_i(t) \quad (2)$$

If  $L$ ,  $C$ ,  $R_L$ ,  $R_C$ , and  $R$  are all assumed linear, the incremental inductor current can be found from Fig. 1 as:

$$\hat{i}_L(s) = G_p(s) \hat{v}_i(s) \quad (3)$$

where  $G_p(s)$  can be given as:

$$G_p(s) = \frac{1 + a_4 s}{a_1 s^2 + a_2 s + a_3} \quad (4)$$

where:

$$a_1 = (R + R_c)LC \quad (5)$$

$$a_2 = (RR_L + R_c R_L + RR_c)C + L$$

$$a_3 = R_L + R$$

$$a_4 = (R + R_c)C$$

The incremental diode voltage can be expressed in terms of the incremental gating function:

$$\hat{v}_i(t) = V_s \hat{h}(t) \quad (6)$$

Jury shows that for the purpose of system analysis, a periodic pulse train can be approximated by a series of impulses with equivalent areas [2]. This approximation is valid if the widths of the pulses are short compared to the period of the pulse train and if the widths of the pulses are also short compared to the time constants of the system. In addition, the pulse train is an input to a linear system.

From Fig. 2 it can be seen that  $\hat{h}(s)$  can be replaced by a series of impulses with areas  $V_s \hat{d}(kT)T$  occurring at times  $kT$  where  $T$  is the switching period in seconds. The function  $\hat{d}(kT)$  is the values of the incremental duty cycle at times  $kT$ . The values for  $\hat{d}(kT)$  can be found by the sampling of the appropriate continuous function  $\hat{d}(t)$ . The approximation for the incremental diode voltage can be written as:

$$\hat{v}_i(t) \approx \sum_{k=0}^{\infty} V_s T \hat{d}(kT) \delta(t - kT) \quad (7)$$

Equation (7) can be written in the Laplace domain as:

$$\hat{v}_i(s) \approx V_s \hat{d}^*(s)T \quad (8)$$

where the asterisk denotes the sampling of a function.

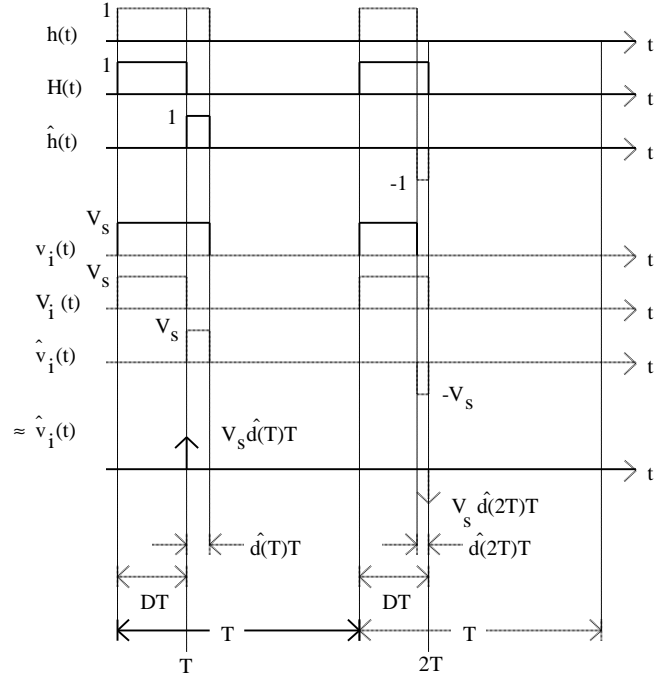


Fig. 2 Impulse approximation.

To complete the model, the effects of perturbances in the control voltage and inductor current on the duty cycle must be derived. This can be derived from the geometry of the waveforms in Fig. 3 and Fig. 4. The rising slope  $m_{on}$  of the inductor current  $i_L(t)$  can be approximated by the difference in the input voltage  $V_s$  and the average, steady-state output voltage  $V_o$  divided by the inductance of  $L$ :

$$m_{on} = \frac{V_s - V_o}{L} \quad (9)$$

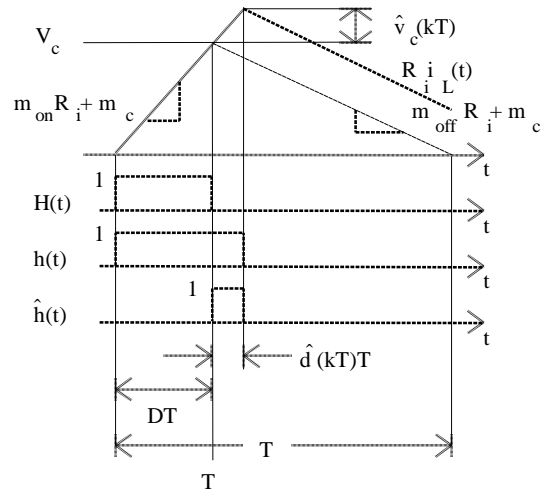


Fig. 3 Duty cycle change due to control voltage.

$R_i$  is the gain of current sensing device in ohms. From the geometry of Fig. 3, the change in the duty cycle due to a change in the control voltage can be derived as:

$$\hat{d}(kT) = \frac{\hat{v}_c(kT)}{(m_{on}R_i + m_c)T} \quad (10)$$

Similarly, from Fig. 4, the change in the duty cycle due to a change in the inductor current can be derived as:

$$\hat{d}(kT) = \frac{-R_i\hat{i}_L(kT)}{(m_{on}R_i + m_c)T} \quad (11)$$

A quantity called the modulator gain can be defined as:

$$F_m = \frac{1}{(m_{on}R_i + m_c)T} \quad (12)$$

From (10), (11), and (12), the following expression may be written:

$$\hat{d}(kT) = F_m [\hat{v}_c(kT) - R_i\hat{i}_L(kT)] \quad (13)$$

From (13), it can be seen that the function  $\hat{d}(t)$  sampled to give  $\hat{d}(kT)$  can be given as:

$$\hat{d}(t) = F_m [\hat{v}_c(t) - R_i\hat{i}_L(t)] \quad (14)$$

Using (3), (8), and (14) the new model for the current-mode controlled buck converter can be drawn as the block diagram in Fig. 5. The blocks in Fig. 5 are defined as follows:

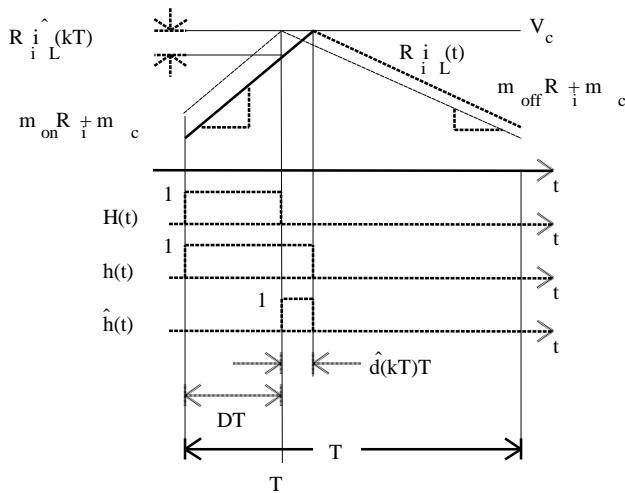


Fig. 4 Duty cycle change due to inductor current decrease.

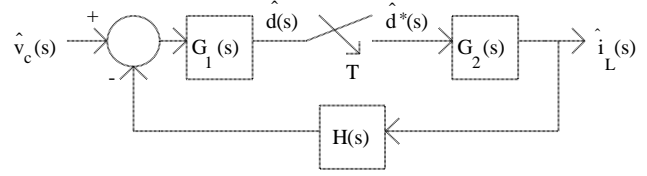


Fig. 5 New model for current-mode controlled buck converter.

$$\begin{aligned} G_1(s) &= F_m e^{-aTs} \\ G_2(s) &= V_s T G_p(s) \\ H(s) &= R_i \end{aligned} \quad (15)$$

Note that a delay  $aT$  that is a *fraction* of the switching period has been introduced into the  $G_1(s)$  block in the model. This distinguishes this model from past sampled-data models. The delay  $aT$  models the delay introduced into the current loop by the control circuitry which is generally a fraction of the switching period. Because of this delay, regular z-transforms can not be used for the evaluation of the loop gain of Fig. 5. Instead, modified z-transforms must be used. Modified z-transforms enable the derivation of system response between the sampling times  $kT$ .

From Fig. 5, the closed-loop transfer function relating the inductor current to the sampled control voltage can be written as [7]:

$$\hat{i}_L(s) = \frac{G_2(s)[G_1(s)\hat{v}_c(s)]^*}{1 + [G_1(s)G_2(s)H(s)]^*} \quad (16)$$

It is seen from (16) that the current loop gain indicative of stability and transient behavior is:

$$L(s) = [G_1(s)G_2(s)H(s)]^* = F_m R_i V_s T [G_p(s)e^{-aTs}]^* \quad (17)$$

Since  $a$  is a fraction of the switching period, modified z-transforms must be used to evaluate (17). The effect of delay on the control loop gain of a non-sampled system is to alter the phase while leaving the magnitude unchanged. In contrast, a delay in a sampled system will alter the magnitude of the loop gain. For a delay less than one sampling period, the z-domain result of a sampled function with a delay may be found by the following equation [2]:

$$(G(s)e^{-aTs})^* = Z_m [G(s)]_{m=1-a} \quad (18)$$

The modified z-transform for a simple pole is given as [2]:

$$Z_m \left[ \frac{1}{s+p} \right] = \frac{e^{-pmT}}{z - e^{-pT}} \quad (19)$$

Using (4), (17), (18), and (19), the following loop gain can be derived in the z-domain:

$$L(z) = k_1 \left[ \frac{(1 + a_4 s_1) e^{s_1 m T}}{z - e^{s_1 T}} - \frac{(1 + a_4 s_2) e^{s_2 m T}}{z - e^{s_2 T}} \right] \quad (20)$$

where:

$$s_{1,2} = \frac{-a_2 \pm (a_2^2 - 4a_1 a_3)^{1/2}}{2a_1} \quad (21)$$

$$k_1 = \frac{F_m R_i V_s T}{a_1 (s_1 - s_2)} \quad (22)$$

$$m = 1 - a \quad (23)$$

If the poles in (20) are not outside the unit circle  $|z| = 1$ , (20) may be transformed into the steady-state frequency domain using the equation [7]:

$$z = e^{j\omega T} \quad (24)$$

This results in the following loop gain:

$$L(j\omega) = k_1 \left[ \frac{(1 + a_4 s_1) e^{s_1 m T}}{e^{j\omega T} - e^{s_1 T}} - \frac{(1 + a_4 s_2) e^{s_2 m T}}{e^{j\omega T} - e^{s_2 T}} \right] \quad (25)$$

A gain and phase plot of (25) can be plotted and investigated for stability information. An indication of instability can indicate the presence of subharmonic oscillations. Due to the presence of the sampler in the new model, it is only necessary to look at the loop gain up to half the sampling frequency [7], which is equal to half the switching frequency  $f_s$ .

Several plots of the loop gain in (25) are shown for various amounts of delay in Fig. 6. Circuit parameters for these plots are shown in Table I. Experimental data taken with the digital modulator are also displayed. It can be seen how not only the phase but the magnitude of the loop gain changes at low frequencies with different amounts of delay. This is in contrast to non-switched circuits where only the phase would be altered. It can also be seen that if the delay is allowed to go to zero, the current loop gain will agree with that predicted by Ridley's model [4].

### III. DIGITAL MODULATOR LOOP GAIN MEASUREMENT

The digital modulator was proposed by Cho and Lee [6] as a method of measuring loop gains in power electronic converters. The waveforms that result from a measurement with the digital modulator are shown in Fig. 7. Two signals  $x(t)$  and  $y(t)$  are generated from the gating waveform  $h(t)$  by the addition of pulses of width  $bT$  seconds. The width  $bT$  is

controlled by the phase and stretch width adjust controls in the digital modulator. The falling edge of  $x(t)$  is then pulse-width modulated by a small sinusoidal signal  $v_m$ . The loop gain is then calculated by the division of  $y(j\omega)$  by  $x(j\omega)$ .

Since the steady-state signals  $X(t)$  and  $Y(t)$  are identical, only the incremental signals  $\hat{x}(t)$  and  $\hat{y}(t)$  will be significant in the loop gain calculation. The signal  $x(t)$  can be viewed as the addition of a train of pulses  $\hat{z}(t)$  added to the signal  $y(t)$ . The pulses  $\hat{z}(t)$  are generated from the pulse-width modulation of the small sinusoidal signal  $v_m$ .

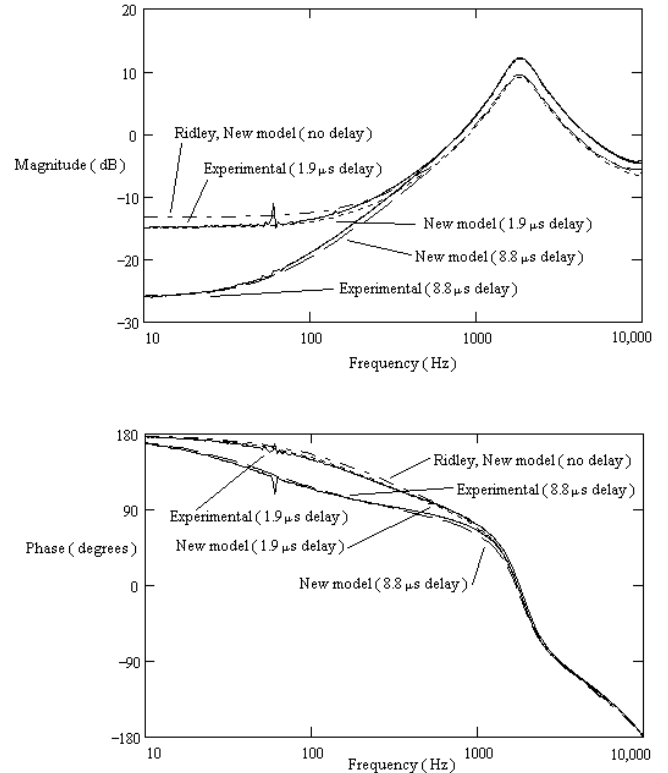


Fig. 6 Theoretical and experimental digital modulator results.

TABLE I

CIRCUIT PARAMETERS FOR FIG. 6.

Parameter	Value	Units
$V_s$	30	V
$V_o$	18	V
$f_s$	20	kHz
$L$	101	$\mu\text{H}$
$R_L$	0.25	$\Omega$
$C$	75	$\mu\text{F}$
$R_c$	0.22	$\Omega$
$R$	7.1	$\Omega$
$R_i$	0.45	$\Omega$
$m_c$	0.073	V/ $\mu\text{s}$

The incremental signal  $\hat{x}(t)$  can then be obtained by the addition of  $\hat{z}(t)$  to the incremental signal  $\hat{y}(t)$ . In addition,  $\hat{y}(t)$  is the result of the incremental signal  $\hat{h}(t)$  delayed by  $bT$  seconds. For small pulsewidths, the signals  $\hat{x}(t)$ ,  $\hat{y}(t)$ ,  $\hat{z}(t)$ , and  $\hat{h}(t)$  can all be approximated by trains of impulses of equivalent areas [2]. Thus, the block diagram for the digital modulator measurement on the current-mode controlled buck converter can be drawn as Fig. 8.

From Fig. 8, the resulting measurement can be derived as [1]:

$$L_{DigMod}(j\omega) = -F_m R_i V_s T \left[ G_p(j\omega) e^{-j\omega(a+b)T} \right]^* \quad (26)$$

It can be seen from (26) that the digital modulator adds an extra delay of  $bT$  seconds into the circuit being measured. It can be seen from (26) that if the delay introduced by the digital modulator approaches zero, then the measurement result will be the desired loop gain (17). Efforts must be made to keep the delay introduced by the digital modulator as small as possible for an accurate current loop gain measurement.

Experimental results confirm the effects of varying amounts of delay introduced by the digital modulator. Fig 6 illustrates the experimental loop gain data obtained with a digital modulator with a  $1.5\mu\text{s}$  delay on a buck converter with a  $0.4\mu\text{s}$  delay. It can be seen that it correlates well with the theoretical loop gain of the new model for a delay of  $1.9\mu\text{s}$ . Also shown is experimental data for the case for a digital modulator with a  $8.4\mu\text{s}$  delay on the same buck converter with  $0.4\mu\text{s}$  of delay. It can be seen that this data correlates well with the theoretical loop gain of the new model for a delay of  $8.8\mu\text{s}$  and also how much  $bT$  of the digital modulator can affect the loop gain measurement.

For this case, the buck converter was operating in continuous conduction mode near the discontinuous conduction mode boundary. Note that the phase angle at low frequencies is at 180 degrees for the parameters in Table I. As the buck converter operates deeper into the continuous conduction mode, the phase angle at low frequencies will shift to zero degrees.

#### IV. CONVENTIONAL LOOP GAIN MEASUREMENT

The conventional loop gain measurements performed on analog circuit has been used on the current-mode controlled buck converter. However, it will be shown that the use of conventional loop gain measurement techniques does not result in the loop gain derived by the new model in (25). To show this, the new model can be used to predict the measurement that will be obtained when conventional measurement techniques are used on the current-mode controlled buck converter.

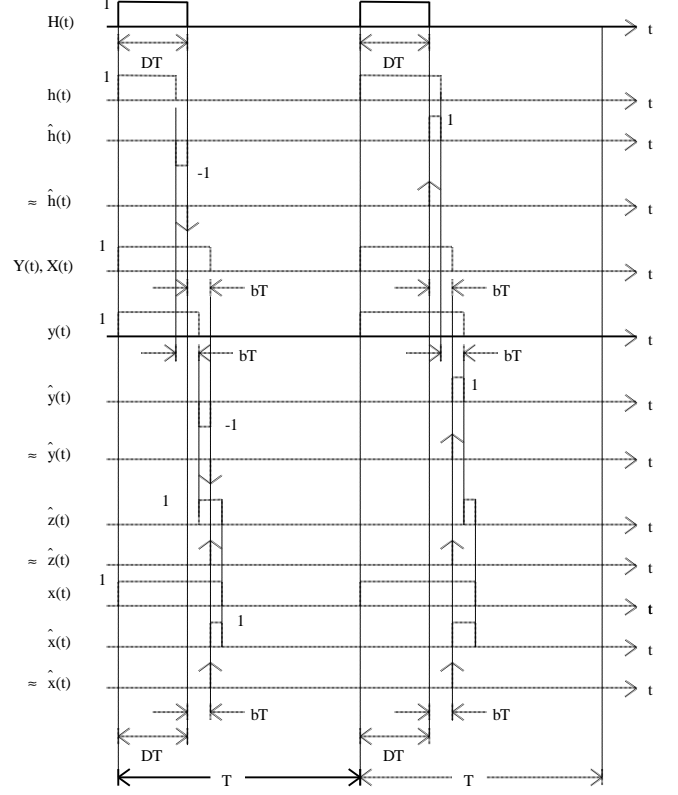


Fig. 7 Digital modulator waveforms.

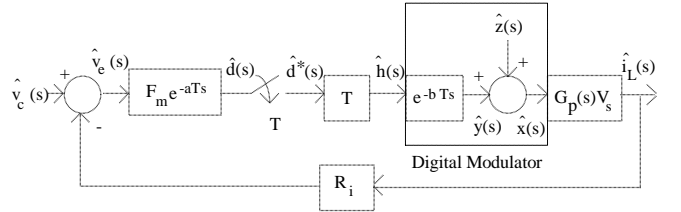


Fig. 8 Equivalent model of digital modulator measurement.

In the use of conventional loop gain measurement techniques for analog circuits, a sinusoidal signal is injected into the control loop [5]. The control loop signal before the injection point divided by the control loop signal after the injection point results in the loop gain of the system. Using the new model, Fig. 9 shows the resulting block diagram that results from the use of a conventional loop gain measurement on the current-mode controlled buck converter. From Fig. 9, it can be shown that the following measurement will be the result [1]:

$$L_{conv}(j\omega) = \frac{-G_1 G_2 H(j\omega)}{T + T \left[ G_1 G_2 H(j\omega) \right]^* - G_1 G_2 H(j\omega)} \quad (27)$$

From (27) it is seen that the conventional measurement does not produce the current loop gain (17) derived from the new model. Fig. 10 illustrates the difference between the experimental conventional measurement and the current loop gain predicted by the new model for the parameters in Table II. Thus, it is shown that the conventional measurement technique does not result in the measurement of the loop gain of the current-mode controlled buck converter. Also shown is how the experimental measurement correlates to the new model's prediction of the conventional measurement given in (27). Shown for comparison is the loop gain predicted by Middlebrook's averaged current-mode control model [8].

### V. CONCLUSION

This proposed modeling procedure describes for the first time the effects of delay introduced by the measurement hardware on the current loop gain of the current-mode controlled buck converter. It is seen that the delay will not only affect the phase of the loop gain but also its magnitude. This effect is especially pronounced when the buck converter is operating in the continuous conduction mode near the discontinuous conduction mode boundary. The total parasitic delay is likely to be significant in many practical applications, and may well account for the discrepancies observed by previous workers in the measured loop gain magnitudes.

It was also demonstrated that the use of conventional loop gain measurement techniques does not result in the measurement of the current loop gain. It is also shown that the use of a digital modulator to measure the loop gain may introduce significant amounts of delay into the circuit being measured. However, if precautions are taken, the introduced delay can be minimized and the digital modulator can be used to obtain a good loop gain measurement.

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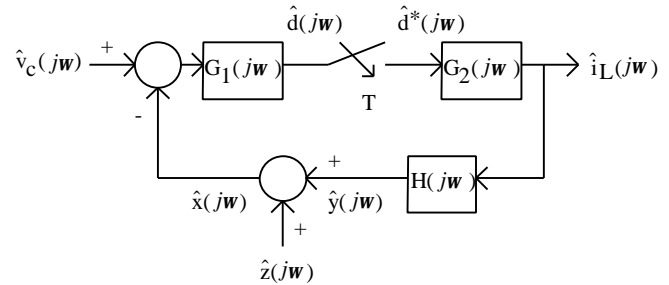


Fig. 9 Conventional measurement of current loop gain.

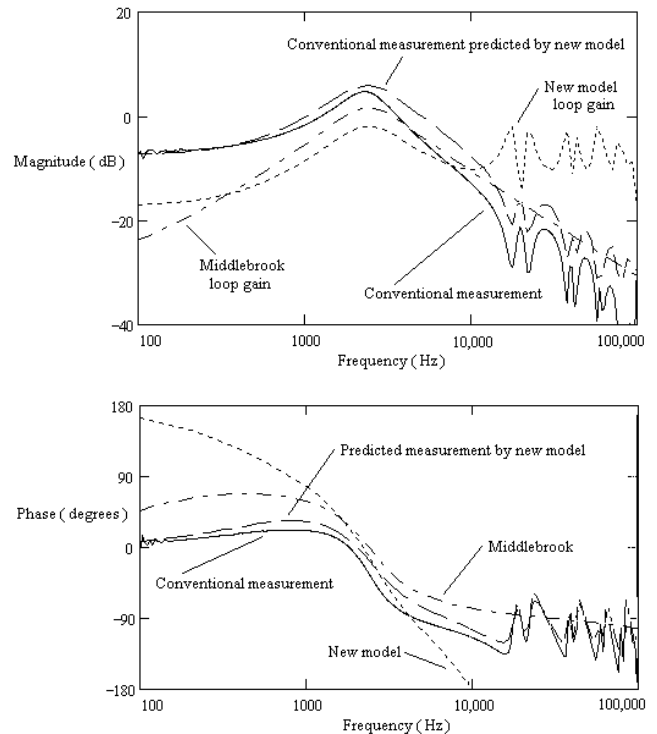


Fig. 10 Conventional measurement of current loop gain.

TABLE II

CIRCUIT PARAMETERS FOR FIG. 10.

Parameter	Value	Units
$V_s$	20.2	V
$V_o$	11.8	V
$f_s$	20	kHz
$L$	101	$\mu\text{H}$
$R_L$	0.25	$\Omega$
$C$	50	$\mu\text{F}$
$R_c$	0.06	$\Omega$
$R$	5.86	$\Omega$
$R_i$	0.55	$\Omega$
$aT$	0.4	$\mu\text{s}$
$m_c$	0.077	$\text{V}/\mu\text{s}$