Guidelines for Digital VLSI Design I Projects

1. Introduction

Term project assignment includes the design, verification, submission for manufacturing, and testing of a basic digital VLSI technology subsystem IC. The goal of projects will be accomplished using the top-down design approach, which will be guided and monitored by a sequence of Phase Reports. Students' work will be helped and supported by the precise requirements and deadlines that need to be met in order for the whole project to be completed successfully on time.

2. Project Work Schedule

Meeting all phase deadlines is important because the manufacturing of the designed chips is scheduled outside of the UT, so the deadline for the submission of the designs for manufacturing can not be changed. The following summary of the Phase Report Preparation Schedule lists the deadlines in terms of the order numbers of the Fall Semester weeks, which are related to the annual calendar in the course Syllabus, which also indicates the day of the week on which the reports are due.

<table>
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<tr>
<th>Phase</th>
<th>Report Topic</th>
<th>Semester week starting</th>
<th>due</th>
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<td>1.</td>
<td>Behavioral description of the project circuit.</td>
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<td>#8</td>
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<td>2.</td>
<td>Architecture, logic design, and floor planning.</td>
<td>#8</td>
<td>#9</td>
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<td>3.</td>
<td>Technology mapping of leaf-cells and logic circuit models on all hierarchical levels. Simulation of circuit models on all levels.</td>
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<td>#11</td>
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<td>4.</td>
<td>Leaf-cell layout design and LVS testing.</td>
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<td>Whole circuit Layout design and LVS testing.</td>
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<td>6.</td>
<td>Framing the core logic and submitting for fabrication.</td>
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<td>7.</td>
<td>Public presentation and defense of the completed designl report.</td>
<td>#8</td>
<td>#17</td>
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<td>8.</td>
<td>Chip test.</td>
<td>chip delivery</td>
<td>a week later</td>
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Progress Reports are due within five minutes of the official beginning time of the class on the due day. Late submissions of progress reports are accepted till the next meeting of the class. This policy is designed to encourage students to attend the class, instead of spending the class time in the lab working on completing a progress report which is due but not yet finished.

3. Procedures

3.1 Design teams

All design work on projects is a team effort. Members of a team are in obligation to share the team’s
effort on an equal basis. Initial differences in opinion between team members are likely to occur, but ought to be resolved within the team in a reasonable time, before a deadline for the submission of a report. In cases when consensus cannot be reached in a reasonable time, the issue must be brought to the attention of the instructor for a final decision. Teams will elect a Team Leader if they can agree on one; otherwise, the instructor will assign that duty to one of the team members.

3.2 Phase Progress reports

It should be understood that the Phase Reports will eventually make the chapters of the Final Project Report. For full credit, all progress reports must be prepared and turned in by the scheduled deadlines, and later kept for reference and inclusion into the final report. The following guidelines specify in general terms the work to be completed. Read them carefully, and see the instructor whenever you need additional information about your particular project. Each Phase report shall have to be defended in front of the teacher during regular office hours. In cases of emergency the instructor will advise students on a walk-in basis, subject to his availability at the time.

3.3 Design Documentation

All handouts, starting with the course syllabus and these Guidelines, as well as homework/Lab assignments, and copies of all material that students are required to turn in, are required to be maintained in a dedicated 'one inch' binder, so that they are available for reference when student comes to defend a Phase Progress Report, a homework/Lab solution, or to seek advice. This requirement is necessary to save students' and instructor's time through better organization. The dedicated one inch binder must be presented at every meeting with the instructor, to qualify the student for the advising/defense. The following guidelines for maintaining the documentation are mandatory, and the team leader is responsible for making sure they are followed.

(a) there is only one 1” binder per project team.
(b) the 1” binder is a depository for the documentation already processed.
(c) new submissions are to be kept outside the 1” binder;
(d) inside the 1” binder:
   - all contents must be attached to the rings of the binder,
   - documents must be arranged in the reverse chronological order, starting from the beginning of the semester,
   - there should not be any material which is not directly required by these Guidelines;
(g) all handouts, and homework assignment turn-ins are considered a part of the project documentation; one sole good copy of each homework/Lab assignment solution should be maintained in the 1” binder.

3.4 Text formatting within the Report

Using the FrameMaker word processor for preparation of reports is required for graduate students. Undergraduate students are strongly encouraged, but not strictly required, to use the FrameMaker
editor. FrameMaker is available from the College of Engineering server on the SUN Stations located in NE-1022 and NE-1026. To assure a professional look of the reports, and save both, the students’ and the instructor’s time, a copy of the Phase Report #1 template file (named f00templ) has been posted on the EECS4610 webpage. Formats of all section headings, figure captions, table headers and text paragraphs must follow those of the Phase Report Template. The easiest way to access them is to import the formats from the template file into the Phase report file. Inside the Phase Report Template, the text in Times New Roman font contains instructions for preparation of the Phase Reports; other text in *italics* is there as a place holder, to present the right view of the document. Additionally, a copy of the first five chapters of the Final Project Report are posted as the "multiphase template" file on the EECS4610 webpage.

### 3.5 Project assignment

Team-specific subsystem projects will be assigned to the design teams in writing by the instructor.

In addition to the team specific subsystems, each team will include into the designed IC a number of ring oscillator modules, such that all I/O pads which are left unused by the designed subsystem are used by ring oscillators.

### 4. Description of Project Phases

#### Phase 1. Behavioral description of the designed subsystem

Goal of the Phase 1:
- understanding what the subsystem to be designed is supposed to do,
- preparation of the behavioral description of the subsystem,
- enumerating input and output signals of the subsystem, and making sure there are no more than 34 of them.

In order to be considered complete the Behavioral Description Report (Phase Report #1) must include:

1.1 black box representation of the circuit (equivalent to entity in VHDL),
1.2 two separate lists, one of the input signal names and the other of the output signal names (designations/labels), both of them alphabetically ordered, followed by the descriptions of their functions; these signal names will be strictly kept unchanged throughout the whole documentation of the project;
1.3 description of the functional relationships between input and output signals,
1.4 an overview of application areas of the subsystem/module.

#### Phase 2. Architecture, logic design, and floorplan design

Goals of the Phase 2:
- understanding one particular implementation of the subsystem, and identify the rest of
modules (submodules) into which the subsystem can be partitioned,
- showing a multi-level hierarchical representation of the circuit,
- creating logic designs of combinational and sequential modules,
- preparing a preliminary floorplan that will show intended physical placement of all modules on the chip surface; this floorplan will serve as a guideline for determining proper aspect ratios of circuit modules in Phase 4.

In order to be considered complete the Architecture, Logic Design, and Floorplan Design Report (Phase Report #2) must include:

2.1 hierarchical representations of logic models of the whole subsystem, and its functional blocks/modules, with the unified terminal designations to be shown on all functional cells in the design,
2.2 black box representations of all modules/cells,
2.3 state and state-transition tables for the sequential modules,
2.4 applied transformations/optimization of the combinational logic functions,
2.5 a drawing of an applicable floorplan design.

Phase 3. Technology mapping: CMOS implementation

Goal of the Phase 3:
- understanding and describing the CMOS implementation of the subsystem leaf cells, including the transistor size optimization issues.

In order to be considered complete the CMOS Implementation Report (Phase Report #3) must include:

3.1 computer generated electric circuit models (schematic diagrams) of all leaf-cell modules that were identified in Phase 2.,
3.2 computer generated logic circuit models (schematic diagrams) of all higher level modules which were identified in Phase 2.,

Hint (a) undergraduate students are strongly encouraged to create these using Mentor Graphics tool, Design Architect; a less desirable alternative tool being SPICE; teacher’s support is available for Design Architect only;
(b) using the Design Architect is mandatory for graduate students.

3.3 Design Architect generated graphical symbols for all leaf-cells,
3.4 Design Architect generated graphical symbols for all higher level modules,
3.5 Check→Sheet→With Defaults reports for the schematics created under 3.1,
3.6 Check→With Defaults reports for all symbols created under 3.3 through 3.4,
3.7 ModelSim generated I/O waveforms from simulations of all leaf-cell electrical models, and higher level logical models developed under 3.1 and 3.2, using
   - the "unit-delay" timing mode,
   - a prepared stimulus file.
3.8 hierarchically unified terminal designations must be provided for all modules in all
documents listed above.

**Phase 4. Layout design and LVS test of leaf cells**

Goals of the Phase 4:
- creating the layout design of subsystem’s leaf-cells, considering how they will be efficiently assembled into the layout of the whole circuit,
- compacting the cell layouts,
- performing the LVS test of the individual cells to verify their proper functioning,
- to not forget including the substrate contacts where appropriate.

In order to be considered complete the **Circuit Modules Layout Report** (Phase Report #4) must include:

4.1 electrical models and layout diagrams of leaf-cells with the unified terminal designations,
4.2 a list of all leaf-cells showing the cell’s: name, length and width, aspect ratio, the area occupied by the cell and the number of transistors in the cell,
4.3 LVS test results for all leaf cells,
4.4 a statement about the functionality of each designed cell that must be made in one of the following two ways:
   - the LVS test result shows that the layout of the cell implements the cell’s circuit, or
   - the LVS test result shows that the layout of the cell does not implements the cell’s circuit.
4.5 a drawing of the finally adopted floorplan design.

**Phase 5. Layout design and LVS test of the whole subsystem**

Goals of the Phase 5:
- assembling the subcircuit modules’ layouts into the complete subsystem layout,
- minimizing the layout area,
- completing the LVS test for subsystem modules on all hierarchical levels, and the top level module,
- making corrections when necessary,
- establishing the correctness of the proper assembly of the whole subsystem.

In order to be considered complete the **Whole Subsystem Layout Design Report** (Phase Report #5) must include:

5.1 logical models and graphical representations of the layout on the module level, and of the whole subsystem,
5.2 LVS test reports for all circuit modules but for those included in the Phase 4 report,
5.3 length, width, aspect ratio, and the area occupied by designed cells and the whole subsystem,
5.4 a statement about the functionality of each designed circuit must be made and signed by all members of a project design team in one of the following two ways:
Phase 6. Framing the core logic and submitting for manufacturing

Goal of Phase 6: To queue in your design for manufacturing at MOSIS.

6.1 Inserting the core logic into the fabrication pad frame

Follow the procedures described in the Version 3.0 ADK manual, the handout Preparing a Completed Core Layout for Manufacturing, and hints provided during classes.

6.2 Converting the framed design to GDS II intermediate form

Follow the procedures described in the Version 3.0 ADK manual, the handout Preparing a Completed Core Layout for Manufacturing, and hints provided during classes.

6.3 Calculating the "crc sum"

- from the course web page, download to your working directory the program mosiscrc.c;
- from a terminal window, compile mosiscrc.c by executing the command:
  > gcc mosiscrc.c -o mosiscrc
- from a terminal window, run the mosiscrc program on your .gds or .cif file:
  > ./mosiscrc -b tlm_<name>.gds
- two numbers will be displayed on the line below the one on which you just typed,
  Checksum: _____________________  Count: _______________
  write down those two numbers carefully, they will be needed in the process of queueing your design for fabrication.

6.4 Obtaining access to the manufacturing account

Due: December 18, 2008
See the course instructor to obtain the design number and password to the account which pays the manufacturing fees.

6.5 Filling out the MOSIS Fabricate form

Due: December 18, 2008

6.5.1 Connect to MOSIS web site using the URL, www.mosis.org.

6.5.2 From the MOSIS home page, use the provided links to navigate to,
  Web Forms → Non secure forms ... → Fabricate
  While there, notice other forms available, especially the CANCELL-FABTICATION form.

6.5.3 Filling out the Fabricate form. The form that pops up has six sections. Students ought to fill out only the first three sections, providing the following data items:
  - Design Number: supplied by the course teacher,
  - Design Password: supplied by the course teacher,
  - Host name of the computer from which the tlm_<name>.gds file will be ftp-ed,
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- Password which will be used for establishing the ftp connection,
- File name of the file to be ftp-ed: \texttt{tlm\_<name>.gds}
- then move to the bottom of the form, and select: Submit.

MOSIS server runs a test on the received form, and almost immediately sends back a report, which may contain:
- warnings and error messages or, in the absence of those, a confirmation that the form successfully passed the test, and that the .gds file may be ftp-ed to MOSIS.

6.6 FTP-ing the .gds file to MOSIS \textbf{MOSIS Absolute Deadline: January 7, 2009}

The report which follows a successful FABRICATE request contains a paragraph with instructions on how to ftp the .gds/.cif file to the MOSIS ftp server. Make sure to understand that the server’s address is: ftp.design.mosis.org, so that your command line looks like this

\texttt{> ftp ftp.design.mosis.org}

Do not forget to do the ftp-ing from the same host, and use the same password that you have entered in the FABRICATE form.

6.7 Receiving the MOSIS response

MOSIS server runs a test on the received .gds file, and almost immediately sends back a MOSIS FTP Report, which may contain:
- warnings,
- error messages,
- a confirmation that the project has successfully passed the test, and that the project has been queued for fabrication.

Print the MOSIS Report. When errors have been found, the FABRICATE form shall have to be executed again, but that will be possible only after the CANCELL-FABTICATION form has been executed. So, in case of errors, execute CANCELL-FABTICATION form immediately to avoid forgetting about it.

\textbf{Hint:} Projects not queued for fabrication by the MOSIS deadline will receive lower grades.

In order to be considered complete the \textbf{Framing the core logic and submitting for manufactureing Report} (Phase Report #6) must include:

6.1 Checksum and Count numbers,
6.2 Design Number,
6.3 Design Password,
6.4 Host name of the computer from which the \texttt{tlm\_<name>.gds} file will be ftp-ed,
6.5 Password which will be used for establishing the ftp connection,
6.6 File name of the file to be ftp-ed: \texttt{tlm\_<name>.gds},
6.7 copy of the MOSIS FABRICATE Report.
6.7 copy of the MOSIS FTP Report.

Goals of Phase 7:
- assembling the Phase-Reports/chapters prepared for the preceding phases,
- preparing the Project Presentation Schedule in the form of the sixth chapter of the Completed Design Report,
- giving a public presentation on the design work/experience to the class,
- all team members, dressed in professional attire, must take part in the presentation on the day, time and place scheduled for the final exam.

In order to be considered complete the **Complete Design Report** (Phase Report #7) must include:

- the first five chapters prepared as the first five Progress reports, as described above,
- the list of contents with page numbers, including the Phase7 and 8 reports placeholders,
- the name and size of the configuration file containing the description of the whole subsystem,
- the Project Presentation Schedule, which must address every section of the project, and must list in the order of presentation:
  a) figure captions of the figures to be shown, with the comments to be made on them (do not forget to start with the behavioral representation),
  b) problems that have been encountered during the design, and how they have been resolved,
  c) remarks specific to the project, including the % of the reduction in the area occupied by the first and last version of the team specific part of the CLM.

**Hint: Porting parts of the reports to PowerPoint:**
- take a snapshot and save it as .rs file,
- open the .rs file in ImageViewer,
- save the file from ImageViewer as .jpg,
- import the .jpg file into PowerPoint.

Phase 8. Testing the manufactured chip

Goal of Phase 8: To establish whether all five IC’s manufactured for your design are fully operational.

When the manufactured chips are delivered, somewhere during the Spring semester, usually six to eight weeks after the submission to MOSIS, a note will be posted on the board next to the instructor’s office. At that time, come and see the instructor for further information about the Lab and the procedures for testing the chip.

Prior to testing the chip’s functionality in the Lab, the team must prepare the testing documentation listed under 8.1 through 8.5 below. Mr Tom Jacob, the EECS Dept. Lab technician, whose office is in NE-1021, will inspect the documentation and provide the test equipment if he finds that the testing procedure is safe for the chip.

In order to be considered complete the **Chip Test report** (Phase Report #8) must include:
8.1 graphical symbol of the chip, with the pin numbers and signals indicated,
8.2 electrical model of the test circuit, showing explicitly all circuit components and connections,
8.3 protoboard layout model of the test circuit, showing exact positions of all components and wires of the test circuit,
8.4 textual description of the testing procedure, addressing the signal levels and timing,
8.5 table with all intended signal inputs, and expected and obtained signal outputs,
8.6 a conclusion section describing the success of the project must include one of the following two statements:
   - "Testing results have shown that the manufactured chip is fully operational."
   - "Testing results have shown that the manufactured chip is not fully operational."
these statements must be dated and signed by all team members.
8.7 in the case when manufactured chip does not work properly, the report must also include the following information:
   - the description of all missing functions,
   - the results of the investigation of the cause(s) for malfunctioning, and
   - a conclusion that states what needs to be changed in the design in order for the chip to become functional.