Term Project Report

VLSI Design of a 16:1 Multiplexer

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               Michael Cassavar
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Chapter 1. Behavioral Description

1.1 Introduction

The main purpose of our project is to design a sixteen to one multiplexer, where a four-bit address selects one of sixteen input signals to a single output signal. An enable signal is used to specify the status of the MUX (Multiplexer) as either enabled or disabled. To implement our project we will use CMOS technology which is primary topic discussed in this course. Several phase reports will be used to document our progress and provide a detailed record of our design. The objective of the first phase is to begin to understand the assigned project, how it functions, and its possible uses.

1.2 Subsystem Interface and I/O signal

The black box representation for 16:1 multiplexer is shown in Figure 1.1, where IN0~IN15 are the pins for sixteen input signals, S0~S3 are the four-bit control signals that determine which input channel is transferred to output pin Y. The EN signal provides external control that can enable or disable the multiplexer. Table 1.1 describes the input signals IN0~IN15, EN, and S0~S3. Table 1.2 lists the description of the output signal Y, and the fourrteen ring oscilator outputs which will be conneced to the I/O pins left unused by the MUX.

![Figure 1.1: Black box representation of the MUX16:1.](image-url)
Table 1.1 List of input signals

<table>
<thead>
<tr>
<th>Order number</th>
<th>Signal name</th>
<th>Description of the signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EN</td>
<td>Enable (logic low)/disable (logic high) control signal</td>
</tr>
<tr>
<td>2</td>
<td>IN0</td>
<td>0th line selection</td>
</tr>
<tr>
<td>3</td>
<td>IN1</td>
<td>1st line selection</td>
</tr>
<tr>
<td>4</td>
<td>IN2</td>
<td>2nd line selection</td>
</tr>
<tr>
<td>5</td>
<td>IN3</td>
<td>3rd line selection</td>
</tr>
<tr>
<td>6</td>
<td>IN4</td>
<td>4th line selection</td>
</tr>
<tr>
<td>7</td>
<td>IN5</td>
<td>5th line selection</td>
</tr>
<tr>
<td>8</td>
<td>IN6</td>
<td>6th line selection</td>
</tr>
<tr>
<td>9</td>
<td>IN7</td>
<td>7th line selection</td>
</tr>
<tr>
<td>10</td>
<td>IN8</td>
<td>8th line selection</td>
</tr>
<tr>
<td>11</td>
<td>IN9</td>
<td>9th line selection</td>
</tr>
<tr>
<td>12</td>
<td>IN10</td>
<td>10th line selection</td>
</tr>
<tr>
<td>13</td>
<td>IN11</td>
<td>11th line selection</td>
</tr>
<tr>
<td>14</td>
<td>IN12</td>
<td>12th line selection</td>
</tr>
<tr>
<td>15</td>
<td>IN13</td>
<td>13th line selection</td>
</tr>
<tr>
<td>16</td>
<td>IN14</td>
<td>14th line selection</td>
</tr>
<tr>
<td>17</td>
<td>IN15</td>
<td>15th line selection</td>
</tr>
<tr>
<td>18</td>
<td>S0</td>
<td>Bit 0 of switch control signal</td>
</tr>
<tr>
<td>19</td>
<td>S1</td>
<td>Bit 1 of switch control signal</td>
</tr>
<tr>
<td>20</td>
<td>S2</td>
<td>Bit 2 of switch control signal</td>
</tr>
<tr>
<td>21</td>
<td>S3</td>
<td>Bit 3 of switch control signal</td>
</tr>
</tbody>
</table>
### Table 1.2 List of output signals

<table>
<thead>
<tr>
<th>Order number</th>
<th>Signal name</th>
<th>Description of the signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Y</td>
<td>Output of the MUX</td>
</tr>
<tr>
<td>2</td>
<td>O3V1</td>
<td>Output of the ring oscillator made of 3 inverters</td>
</tr>
<tr>
<td>3</td>
<td>O5V1</td>
<td>Output of the ring oscillator made of 5 inverters</td>
</tr>
<tr>
<td>4</td>
<td>O7V1</td>
<td>Output of the ring oscillator made of 7 inverters</td>
</tr>
<tr>
<td>5</td>
<td>O9V1</td>
<td>Output of the ring oscillator made of 9 inverters</td>
</tr>
<tr>
<td>6</td>
<td>O11V1</td>
<td>Output of the ring oscillator made of 11 inverters</td>
</tr>
<tr>
<td>7</td>
<td>O3V2</td>
<td>Output of the ring oscillator made of 3 inverters</td>
</tr>
<tr>
<td>8</td>
<td>O5V2</td>
<td>Output of the ring oscillator made of 5 inverters</td>
</tr>
<tr>
<td>9</td>
<td>O7V2</td>
<td>Output of the ring oscillator made of 7 inverters</td>
</tr>
<tr>
<td>10</td>
<td>O9V2</td>
<td>Output of the ring oscillator made of 9 inverters</td>
</tr>
<tr>
<td>11</td>
<td>O11V2</td>
<td>Output of the ring oscillator made of 11 inverters</td>
</tr>
<tr>
<td>12</td>
<td>O21V2</td>
<td>Output of the ring oscillator made of 21 inverters</td>
</tr>
<tr>
<td>13</td>
<td>O21V1</td>
<td>Output of the ring oscillator made of 21 inverters</td>
</tr>
</tbody>
</table>

### 1.3 Functional description: I/O relations of the main subsystem module

A 16x1 MUX reads in a four-bit control signal whose value determines the data output Y selected from one of sixteen data inputs. The EN control signal is utilized to enable or disable the MUX. In order to prevent the device from interfering with the output data signal bus, it is important that when the enable input signal is high that a high-impedance state is placed on the data output.

### 1.4 Areas of application of the main subsystem

A 16x1 multiplexer can serve multiple purposes. For example, it can be used to reduce signals from multiple data devices down to a single data path. It can also be used to convert parallel data to serial data if an internal clocking signal is provided. In general, a MUX can be used in any number of applications including audio, video, or digital signal processing.
Chapter 2. Architecture, Design Description and Floorplan

2.1 Introduction

During the last phase of our report we described how our 16:1 MUX functions, its input/control signals and its outputs and their purposes. In this section, we will begin to describe how our 16:1 MUX functions by breaking it down into basic parts and describing each of their functions. We will describe these parts by defining their architecture, providing a basis for their design, and finally providing a general floor-plan layout. By the end of this section, we will have a better understanding of hierarchy, each step’s function in the providing desired output, and how each step functions in complete circuit.

2.2 Architecture

In the simpler design, for example 2:1 multiplexer, we implement the functionality very simply with two transmission gates. For more complex multiplexers, we can think of them as being multiple 2:1 multiplexers in cascade. To implement our 16:1 multiplexer we will use a 4:1 multiplexer as the basis for our cascading design. By doing this, we break design down into manageable parts. The reason we choose 4:1 multiplexer, as opposed to other multiplexers, for the basis hierarchy is because it reduces the complexity of the whole circuit while retaining the ability to re-use the same basic component. Figure 2.1, below, shows how the 16:1 multiplexer is constructed using 4:1 multiplexers. One buffer module is also applied to pull up the voltage level wasted by the transmission gates in the previous stages.

![Figure 2.1 Sixteen-to-one multiplexer. (a) Black box representation. (b) Architecture.](image)

As discussed in chapter one, our multiplexer design uses the EN signal to allow us to disable the multiplexer. This functionality is represented in the hierarchy as MSO (module for signal output). MSO is a very simple part of the hierarchy which enables us to control the output signal by allowing the multiplexer’s output to conduct or be set to high impedance state. Next we will take a closer look at some of the details of our design.
2.3 Design Description

The design of a multiplexer can be accomplished in one of two ways, either by logic or implementation through transmission gates. Our design will be implemented using transmission gates which is specified by the requirements of our project.

As mentioned in section 2.1, an architecture of the whole design should be developed first. Using Table 2.1, truth table of the 16:1 multiplexer, the designer should be able to derive logic expression for output Y. The designer should follow all the correct logical deriving and simplifying methods in order to achieve a minimal and in that manner better design.

In Table 2.1, output signal column (Y) should be expressed as presented in the truth table. S3, S2, S1, S0 are the selection control signal that determine which channel is selected to the output side. EN is enable control signal that makes sure the 16:1 multiplexer release bus control if it is not selected. When enable control signal EN is set high, the output signal is put in high impedance status "Z*". "X" means DON'T CARE status, and no indication is needed for such state. Output "INn" means the nth channel signal is selected.

<table>
<thead>
<tr>
<th>EN</th>
<th>S3</th>
<th>S2</th>
<th>S1</th>
<th>S0</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Z*</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>IN0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>IN1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>IN2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>IN3</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>IN4</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>IN5</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>IN6</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>IN7</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>IN8</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>IN9</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>IN10</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>IN11</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>IN12</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>IN13</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>IN14</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>IN15</td>
</tr>
</tbody>
</table>
In the following paragraphs, the output signal Y is derived in detail.

\[ Y = \overline{E} \overline{N} (S_3' S_2' S_1' S_0' I_0 + S_3' S_2' S_1' S_0 I_1 + S_3' S_2 S_1' S_0' I_2 + S_3' S_2 S_1 S_0' I_3 + S_3' S_2 S_1 S_0 I_4 + S_3 S_2' S_1' S_0' I_5 + S_3 S_2 S_1' S_0 I_6 + S_3 S_2 S_1 S_0' I_7 + S_3 S_2 S_1 S_0 I_8 + S_3 S_2' S_1' S_0 I_9 + S_3 S_2' S_1 S_0' I_{10} + S_3 S_2' S_1 S_0 I_{11} + S_3 S_2 S_1' S_0' I_{12} + S_3 S_2 S_1' S_0 I_{13} + S_3 S_2 S_1 S_0' I_{14} + S_3 S_2 S_1 S_0 I_{15}) \quad (2-1) \]

\[ Y = \overline{E} \overline{N} (S_3' S_2' (S_1' S_0' I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3) + S_3' S_2 (S_1' S_0' I_4 + S_1' S_0 I_5 + S_1 S_0' I_6 + S_1 S_0 I_7) + S_3 S_2' (S_1' S_0' I_8 + S_1' S_0 I_9 + S_1 S_0' I_{10} + S_1 S_0 I_{11}) + S_3 S_2 (S_1' S_0' I_{12} + S_1' S_0 I_{13} + S_1 S_0' I_{14} + S_1 S_0 I_{15})) \quad (2-2) \]

We use five intermediate variables to denote the partial logic functions, then the output signal can be expressed in brief.

\[ DS_0 = S_1' S_0' I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3 \quad (2-3) \]
\[ DS_1 = S_1' S_0' I_4 + S_1' S_0 I_5 + S_1 S_0' I_6 + S_1 S_0 I_7 \quad (2-4) \]
\[ DS_2 = S_1' S_0' I_8 + S_1' S_0 I_9 + S_1 S_0' I_{10} + S_1 S_0 I_{11} \quad (2-5) \]
\[ DS_3 = S_1' S_0' I_{12} + S_1' S_0 I_{13} + S_1 S_0' I_{14} + S_1 S_0 I_{15} \quad (2-6) \]
\[ DS_4 = S_3' S_2' DS_0 + S_3' S_2 DS_1 + S_3 S_2' DS_2 + S_3 S_2 DS_3 \quad (2-7) \]
\[ Y = \overline{E} \overline{N} DS_4 \quad (2-8) \]

The equations from (2-3) to (2-7) can be realized in steering logic as a 4:1 multiplexer, and one transmission gate expressing equation (2-8).

In Figure 2.2, 4:1 MUX module realizes the function \( Y = \overline{M}_S \overline{M}_S D_0 + \overline{M}_S M_S D_1 + M_S \overline{M}_S D_2 + M_S M_S D_3 \) a 4:1 multiplexer in switching logic.

Thus we can consider all multiplexers (two columns of 4:1MUXs on the left side in Figure 2.1) utilizing control signals S0 and S1, as first stage multiplexers, equations (2-3) to (2-6). A second stage multiplexer (4:1MUX on the top right side in Figure 2.1) then is used to reduce the four first stage
multiplexers down to a single output, equation (2-7). Equation (2-8) again acts as a single transmission gate using control signal $\overline{EN}$ to set a high impedance state on the output when desired. One buffer module is used to pull up the voltage level lowered down by the four cascades of transmission gates that are not supported by their own power sources, as each 4:1MUX module has two cascades of transmission gates, totally five transmission gates. These segments are taken from the basis of our architecture in the previous section.

In Figure 2.3, BUF module is one buffer that makes sure the signal magnitude is high enough to be transmitted to next stage, and it is composed of two inverters.

![Buffer module MBUF](image)

Figure 2.3 Buffer module MBUF. (a) Black box presentation. (b) Architecture

In Figure 2.4, TSO module realizes the function $Y = A \overline{EN}$, which is composed of one transmission gate and one inverter.

![Signal output module TSO](image)

Figure 2.4 Signal output module TSO. (a) Black box presentation. (b) Architecture.
2.4 Floor-plan Design

As the final part of this chapter we will briefly discuss the floor-plan layout we intend to use. From what we know now about the circuit it is a little difficult to state exactly which layout would be best. For the floor-plan we aim for a layout plan which is simple and practical for our ultimate chip design.

Figure 2-4 is the floor-plan designation for the 16:1 multiplexer, and it consists of two rows and three columns of sub-modules, five of which are channel selection modules 4:1MUX that are connected to the output interface by module TSO. The 16:1 multiplexer is a combinational circuit that is formed of transmission gates.

![Floor-plan of 16:1 multiplexer.](image)

Figure 2.5 Floor-plan of 16:1 multiplexer.
Chapter 3. Technology Mapping: CMOS Implementation

3.1 Introduction

The goal of this section is to begin develop the circuit for implementation in CMOS technology. For this we need to identify each leaf cell shown in the previous chapter. We will then proceed to develop the electrical model for these cells. Each of these cells will need to be verified by simulating their results in either the Design Architect Suite or P-Spice. Using these basic components we will then proceed to create diagrams for each higher level module and create symbols for them as well. By the end of this phase we will have provided a basis for the complete electrical design in terms of the leaf cells and the modules they are used to create.

3.2 Inverter Leaf-Cell

Figure 3.1 shows the Architect generated graphical logic symbol and the electric circuit module for the inverter in CMOS technology, presenting "A" as an input signal and "Y" as an output signal.

As you can see, this leaf cell is very straight forward, and by no means an original design for our project. It is the use of these cells that define our design, and not the cells themselves. These are very simple and should not require much explanation as they can easily be located in almost any reference.

As can be seen in the simulation result included in the previous figure, the electrical model developed for the inverter does provide the desired result.
### 3.3 Transmission Gate Leaf-Cell

Figure 3.2 shows the graphical symbol, electrical model, and simulation results of the transmission gate. Again the functionality of the transmission gate is very clear.

![Figure 3.2 Transmission gate.](image)

(a) Graphical symbol. (b) Electrical model. (c) Simulation waveforms.

### 3.4 BUF Module

Next we will present a common symbology for examining our design and referencing higher level components. Much of this design was accomplished in the previous phases, when specified each of our higher level modules which form the architecture function with respect to circuit implementation. The only real difference for this phase is that we have taken these components and implemented them in Design Architect for later simulation. Figure 3.3 shows our next part which is the buffer, used to step up the voltage level after going through our multiplexers, before reaching the output.
3.5 TSO Module

The TSO module acts to set a high impedance state on the output when the control signal EN is logic high. Figure 3.4 again shows the graphical symbol for this module, its architecture, and simulation results. In Figure 3.4(c), C’ is the EN signal.
3.6 MUX4:1 Module

Our 4:1 multiplexor serves as the basis to developing our 16:1 multiplexor. Below, Figure 3.5, includes the graphical symbol, architecture, and simulation results for this module.

Figure 3.5 4:1 Multiplexor. (a) Graphical symbol. (b) Architecture. (c) Simulation waveforms.
3.7 MUX16:1 Module

Figure 3.6 shows our 16:1 multiplexor. This is our highest level module as represents the complete hierarchy. Finally we have included the graphical symbol, architecture, and simulation results.

Figure 3.6 16:1 Multiplexor. (a) Graphical symbol. (b) Architecture. (c) Simulation waveforms.
Chapter 4: Physical Design of the Circuit’s Modules

4.1 Introduction

The goal of this chapter is to show the layout designs of our leaf cells, the inverter gate and transmission gate. Sections 4.2 and 4.3 show the physical layout of an inverter and a transmission gate respectively. All designs have been created using CMOS scalable technology in terms of lambda. Section 4.4 contains a table that provides some general information about the leaf cell layouts. Lastly we will discuss our finalized floorplan layout.

4.2 Inverter Gate

The electrical model and physical layout of the inverter gate are shown in Figure 4.1 (a), (b) respectively.

![Inverter gate diagram](image)

**Figure 4.1 Inverter gate.** (a) Electrical model. (b) Physical layout.

Inverter gate layout and its electrical model have passed the LVS test, and the LVS report is listed as follows.
REPORT FILE NAME:         /home/top/zhwang/wzh/vlsi/mgc2/lvs.rep
LAYOUT NAME:              /home/top/zhwang/wzh/vlsi/mgc/InverterGate_Layout3
SOURCE NAME:              /home/top/zhwang/wzh/vlsi/mgc2/Inverter_E/ami05a
RULE FILE:                /eng/applications/mentor/adk3_0/technology/ic/process/ami12.rules
LVS MODE:                 Mask
RULE FILE NAME:           /eng/applications/mentor/adk3_0/technology/ic/process/ami12.rules
CREATION TIME:            Wed Nov  9 13:30:38 2005
CURRENT DIRECTORY:        /home/top/zhwang/wzh/vlsi/mgc2
USER NAME:                zhwang
*****************************************************************************
OVERALL COMPARISON RESULTS
*****************************************************************************
#       ###################       _   _
#        #                            #       *   *
#   #        #     CORRECT        #           |
# #         #                            #       \
#           ###################
--------------------------------------------------------------------------------------------------------------
NUMBERS OF OBJECTS
------------------

<table>
<thead>
<tr>
<th>Layout</th>
<th>Source</th>
<th>Component Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ports:</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Nets:</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Instances:</td>
<td>1</td>
<td>mn (4 pins)</td>
</tr>
<tr>
<td>1</td>
<td>mp (4 pins)</td>
<td></td>
</tr>
<tr>
<td>Total Inst:</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

“The Simulation results show that the designed circuit is fully functional”
4.3 Transmission Gate

The electrical model and physical layout of the transmission gate are shown in Figure 4.2 (a), (b) respectively. LVS check has not been performed for the leaf-cell, but will be verified in next phase higher level modules. This is due to an error in the IC Station which requires substrate contacts even though none are needed.

(a)

(b)

Figure 4.2 Transmission gate. (a) Electrical model. (b) Physical layout.
4.4 Dimensions of Leaf Cells

All dimensions of leaf cells (inverter and transmission gate), length width, aspect ratio, area occupied and number of transistors are presented in Table 4.1.

Table 4.1 Dimensions of leaf cells.

<table>
<thead>
<tr>
<th>Cell Name</th>
<th>Length [λ]</th>
<th>Width [λ]</th>
<th>Aspect Ratio</th>
<th>Area [λ²]</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>32</td>
<td>27.5</td>
<td>1.16</td>
<td>880</td>
<td>2</td>
</tr>
<tr>
<td>Transmission gate</td>
<td>32</td>
<td>29</td>
<td>1.10</td>
<td>928</td>
<td>2</td>
</tr>
</tbody>
</table>

4.5 Finalized Floor Plan Layout

As presented in phase two, our floor plan layout is unchanged. There does not appear to be any issue with the previous floor plan design whose merit might change. Therefore the floor plan presented here (Figure 4.3) is unchanged from the previous in phase two.

Figure 4.3 The final design floor-plan of 16:1 multiplexer.
Chapter 5: Physical Design of the Whole Circuit

5.1 Introduction

In phase 3, the simulation results have proved the functionality of all modules, and the layout of leaf cells including inverter and transmission gate is also provided in phase 4. In this chapter, the graphical representations of the layout of module levels are provided, and finally all sub circuit modules are assembled to final whole circuit layout. The LVS test results are also provided for each module architecture and layout.

5.2 MUX4:1 Module

The electrical model and physical layout of the 4:1MUX are shown in Figure 5.1 (a), (b) respectively. Also included below is the LVS report generated by IC station.

![Figure 5.1 MUX4:1 Module.](image)

(a) Architecture. (b) Physical Layout.
The Simulation results show that the designed circuit is fully functional
5.3 BUF Module

The electrical model and physical layout of the BUF module are shown in Figure 5.2 (a) and (b) respectively. Also listed below is the LVS report generated for the BUF module.

![Figure 5.2 BUF Module. (a) Architecture. (b) Physical Layout.](image-url)
REPORT FILE NAME:         /home/top/mcassava/lvs.rep
LAYOUT NAME:              /home/top/mcassava/buffer
SOURCE NAME:              /home/top/mcassava/VLSI/PROJ/BUF/ami05a
RULE FILE:                /eng/applications/mentor/adk3_0/technology/ic/process/ami12.rules
LVS MODE:                 Mask
RULE FILE NAME:           /eng/applications/mentor/adk3_0/technology/ic/process/ami12.rules
CREATION TIME:            Tue Nov 29 17:36:00 2005
CURRENT DIRECTORY:        /home/top/mcassava
USER NAME:                mcassava

**********************************************************************
OVERALL COMPARISON RESULTS
**********************************************************************

#       ###################       _   _
#        #                            #       *   *
#   #         #     CORRECT        #          |
# #          #                            #       \
#            ###################
--------------------------------------------------------------------------------------------------------------

NUMBERS OF OBJECTS

<table>
<thead>
<tr>
<th>Layout Source</th>
<th>Component Type</th>
</tr>
</thead>
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<tr>
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<td>4 4</td>
</tr>
<tr>
<td>Nets:</td>
<td>5 5</td>
</tr>
<tr>
<td>Instances:</td>
<td>2 2 mn (4 pins)</td>
</tr>
<tr>
<td></td>
<td>2 2 mp (4 pins)</td>
</tr>
<tr>
<td>Total Inst:</td>
<td>4 4</td>
</tr>
</tbody>
</table>

“The Simulation results show that the designed circuit is fully functional”
5.4 TSO Module

The electrical model, physical layout of the TSO module are shown in Figure 5.3 (a) and (b) respectively. Also listed below is the LVS report generated for the TSO module.

Figure 5.3 TSO Module. (a) Architecture. (b) Physical Layout.
REPORT FILE NAME:       /home/top/mcassava/lvs.rep
LAYOUT NAME:             /home/top/mcassava/TSO
SOURCE NAME:            /home/top/mcassava/VLSI/PROJ/TSO/ami05a
RULE FILE:              /eng/applications/mentor/adk3_0/technology/ic/process/ami12.rules
LVS MODE:               Mask
RULE FILE NAME:         /eng/applications/mentor/adk3_0/technology/ic/process/ami12.rules
CREATION TIME:          Tue Nov 29 17:39:22 2005
CURRENT DIRECTORY:      /home/top/mcassava
USER NAME:              mcassava

*****************************************************************************
OVERALL COMPARISON RESULTS
*****************************************************************************

NUMBERS OF OBJECTS

<table>
<thead>
<tr>
<th>Layout Source</th>
<th>Component Type</th>
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<td>Nets:</td>
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<td>Instances:</td>
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<td>2</td>
<td>2</td>
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<td>2</td>
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<td>Total Inst:</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

“The Simulation results show that the designed circuit is fully functional”
5.5 MUX16:1 Top Module

The electrical model and physical layout of the 16:1MUX are shown in Figure 5.4 (a) and (b) respectively. Also included below is the LVS report generated by IC station.

Figure 5.4 16:1MUX. (a) Electrical Model. (b) Physical Layout.
REPORT FILE NAME:        /home/top/mcassava/lvs.rep
LAYOUT NAME:              /home/top/mcassava/16x1-2
SOURCE NAME:              /home/top/mcassava/VLSI/PROJ/16x1MUX/ami05a
RULE FILE:                /eng/applications/mentor/adk3_0/technology/ic/process/ami12.rules
LVS MODE:                 Mask
RULE FILE NAME:           /eng/applications/mentor/adk3_0/technology/ic/process/ami12.rules
CREATION TIME:            Sun Dec 4 17:46:35 2005
CURRENT DIRECTORY:        /home/top/mcassava
USER NAME:                mcassava

OVERALL COMPARISON RESULTS

NUMBERS OF OBJECTS

<table>
<thead>
<tr>
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<th>Component Type</th>
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</thead>
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<td>52 52</td>
</tr>
<tr>
<td>Instances:</td>
<td>44 44 mn (4 pins)</td>
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<tr>
<td></td>
<td>44 44 mp (4 pins)</td>
</tr>
<tr>
<td>Total Inst:</td>
<td>88 88</td>
</tr>
</tbody>
</table>

“The Simulation results show that the designed circuit is fully functional”
5.6 Dimensions of the Subsystem Modules and the Whole Circuit

The length, width, aspect ratio and area occupied by the subsystem modules and the whole circuit are shown in Table 5.1.

Table 5.1: Dimensions of Subsystem Modules.

<table>
<thead>
<tr>
<th>Cell Name</th>
<th>Length [(\lambda)]</th>
<th>Width [(\lambda)]</th>
<th>Aspect Ratio</th>
<th>Area occupied [(\lambda^2)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>MUX4:1</td>
<td>135</td>
<td>100</td>
<td>1.35</td>
<td>13500</td>
</tr>
<tr>
<td>BUF</td>
<td>80</td>
<td>45</td>
<td>1.78</td>
<td>3600</td>
</tr>
<tr>
<td>TSO</td>
<td>80</td>
<td>55</td>
<td>1.45</td>
<td>4400</td>
</tr>
<tr>
<td>MUX16:1</td>
<td>400</td>
<td>210</td>
<td>1.90</td>
<td>84000</td>
</tr>
</tbody>
</table>

5.7 Conclusions

Due to our redesign of our layout for our second submission we were able to save area in both the 4:1 Multiplexor cell and the final layout, by altering the layout of our transistors. The area required for our new 4:1 Multiplexor is 35% less than it was originally. This savings transfers over to the final layout which had a shrinkage of 48%. The area now required for our final layout is roughly 1/2 of what it was before.
Chapter 7. Framing the Core Logic and submitting final design

7.1 Introduction
This is the last phase in circuit designing before the designs are finally submitted to MOSIS for manufacturing. It involves generation of pad frame, inserting final layout of the D register into the frame and then drawing out connections of all input and output signals to the pad frame. Finally the pad frame structure is reduced to 0.8 scale as MOSIS follows 1.5micron design. The GDS II file is created which is file to be submitted to MOSIS. This phase gives a detailed view of all the mentioned steps.

7.2 Framing the Core Logic
Once the final layout was completed, it had to be put into a Pad frame which is used to connect the internal signals to the exterior pins. The Pad frame generation was done by first developing the schematic for the IO pads along with the TLM as shown in figure 7.1

![Pad Frame schematic with TLM.](image)

The layout for the pad frame was generated using ADK and the connections were made using metal1 and metal2 as seen in the above schematic. Figure 7.2 shows the layout of the pad frame.
The pad frame was then scaled down by ADK 1.5 micron rule to 0.8. This scaled Pad frame is now used in the generation of the GDS II file.

An important point in the pad frame to be noticed is that there is another layout within pad frame along with the main cell. The other layout is of a Ring oscillator which is formed by series connection of odd number of inverters, with the output of the last inverter being fed back as the input. Its main purpose is to help to analyze rise and fall times. The logical model and layout of the ring oscillator is shown in figure 6.3(a) and 6.3(b)

Figure 7.2 Pad Frame schematic with TLM.
REPORT FILE NAME: /home/top/pbhadav/dvsl1/ringoec.lvs.rep
LAYOUT NAME: $MOC_MD/ringoec
SOURCE NAME: $MOC_MD/ringoec/lvs
RULE FILE: /eng/applications/mentor/adk3.0/technology/ic/process/am112.rules
LVS MODE: Mask
RULE FILE NAME: /eng/applications/mentor/adk3.0/technology/ic/process/am112.rules
CREATION TIME: Wed Dec 7 14:43:59 2005
CURRENT DIRECTORY: /home/top/pbhadav/dvsl1
USER NAME: pbhadav

OVERALL COMPARISON RESULTS

NUMBERS OF OBJECTS AFTER TRANSFORMATION

<table>
<thead>
<tr>
<th>Layout</th>
<th>Source</th>
<th>Component Type</th>
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</tr>
<tr>
<td>Total Inst:</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

INFORMATION AND WARNINGS

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<tr>
<th>Matched Layout</th>
<th>Matched Source</th>
<th>Unmatched Layout</th>
<th>Unmatched Source</th>
<th>Component Type</th>
</tr>
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<tr>
<td>Instances:</td>
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</tr>
<tr>
<td>Total Inst:</td>
<td>3</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Initial Correspondence Points:

Ports: VDD QND Z

SUMMARY

Total CPU Time: 0 sec
Total Elapsed Time: 0 sec

1/8/07
7.3 Generating the GDS II file

The GDS II file is generated by clicking on IClink in the ADK software. The source for such file is ICgraph or layout of the scaled pad frame and destination is the GDS II file of name JKreg.gds. Once this file is generated, a program mosiscrc is run to obtain the CRC and Checksum values for the GDS file.

The generated CRC-Checksum and the count values were:
- checksum: 3350107300
- count: 784690

7.4 Generating the assumed bonding pattern for the manufactured IC

In preparation for testing the manufactured chip, the following two drawings shown in Figure 7.3 have been prepared:
- the sketch of the I/O signal connections to the pads of the frame, shown in Figure 7.3(a),
- the assumed bonding pattern signal connections to the pins of the DIP40 IC package, shown in Figure 7.3(b).

Figure 7.3 Assumed MOSIS Bonding pattern. (a)Connections of signals to bonding pads. (b) DIP40 package signal-to-pin connections.
Chapter 7. Project Presentation Schedule

Introduction About VLSI Designing

Topics covered in the Presentation

   Behavioral Description
   Architectural Designing and Floor Planning
   Technology Mapping
   Leaf Cell Designing
   Whole Circuit Designing

Phase1: Behavioral Description

   Black Box Representation
   Functional description along with truth table

Phase2: Architecture, Logic and Floor Plan Design

   Final architecture of D register
   Black Box representation of modules and submodules
   Floor plan design

Phase3: Technology Mapping

   Electrical schematics of leaf cells along with their simulations.
   Logical module and simulation of D flipflop.

Phase4: Physical Design of Leaf cells

   Electrical schematic and layouts of leaf cells

Phase5: Physical design of higher level modules

   Logical design along with the layout for higher level modules.
   Layout reduction by use of metal 2
   LVS testing
   Layout of whole D register
   Applications of the subsystem
Chapter 8. Testing the manufactured chip

8.1 Introduction

This report describes the procedure to be used for testing the manufactured chip. The report consists of the graphical symbol of the chip with pin assignments for the different signals, an electrical model of the test circuit showing all connections to the chip. It will also give a detailed textual description of the testing procedure.

8.2 Graphical Symbol of the chip

Figure 8.1 shows the graphical symbol of the chip with the pin numbers and appropriate signals indicated.

In the Figure 8.1 the signals indicated as NC are unconnected pins which have no signal assignments.
8.3 Connections of the test circuit and the chip

Figure 8.2 represents the various connections of the test circuit to the chip.

![Test circuit diagram]

8.4 Textual description of the testing procedure

8.4.1 Basic Connections

The fabricated chip is mounted on the bread board. The bread board has in-built GND and VDD connections. At one side of the bread board there are input-output LED indicators with switches. Whenever the LED is on, it represents the logic 1, while LED in off state represents logic 0 for that input/output. The input/output connections are made with the help of the wires. One end of the wire is connected to the pin of fabricated chip and other end is connected to LED on/off switch. The GND and VDD pins are connected to GND and VDD of the board. Clock input to the chip is given with help of function generator. Clear (CLR) and preset (PR) inputs are connected to either logic 0 or logic 1 depending on whether we want to clear or preset the flip-flops.
8.4.2 Test Procedure for a single D flip-flop

**Part I: Clearing/setting of flip-flop**

Step 1: D1 (pin 15) is connected to input switch. This input switch can be set at any position, either logic 1 or logic 0.

Step 2: Clock of 1 Hz frequency is set using function generator. CLK (pin 21) is connected to clock generator output.

Step 3: CLR (pin 22) is connected to GND of bread board.

Step 4: Z1(pin 14) is connected to output LED. Output LED in off state ensures clearing of the flip-flop.

Step 5: Once clearing of flip-flop is ensured, CLR (pin 22) is disconnected from GND and connected to VDD of bread board. PR (pin 1) is connected to GND of bread board.

Step 6: Output LED in on state ensures the setting of flip-flop.

**Part II: Checking the functional behavior of flip-flop**

Step 1: Both CLR (pin 22) and PR (pin 1) are connected to VDD of bread board.

Step 2: D1 (pin 15) is connected to input switch. This input switch can be set at any position, either logic 1 or logic 0.

Step 3: Clock of 1 Hz frequency is set using function generator. CLK (pin 21) is connected to clock generator output.

Step 4: Z1(pin 14) is connected to output LED.

After all these settings the functional behavior of D flip-flop is checked with the help of truth table shown below.

<table>
<thead>
<tr>
<th>PR</th>
<th>CLR</th>
<th>D</th>
<th>CLK</th>
<th>Expected Z</th>
<th>Observed Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
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<tr>
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<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 8.1 Truth table for the D flip flop.

The same test procedure is repeated for remaining seven D flip-flops.

**Part III: Testing the Ring Oscillator output**
The Ring oscillator output on chip (pin 40) is connected to oscilloscope input channel for verification.

8.5 Test Results

Part I: Clearing/setting of flip-flop

The testing routine was carried out as mentioned in the Step 1 through Step 6 of the article 8.3.2 described above. The results were satisfactory.

Part II: Checking the functional behavior of flip-flop

The testing routine was carried out as mentioned in the Step 1 through Step 4 of the article 8.3.2 d

Part III: Testing the Ring Oscillator output

The Ring oscillator output on chip (pin 40) was connected to oscilloscope input channel and the square wave was observed.

8.6 Conclusion

A statement regarding the conclusion of the designed circuit can be made

" Testing results have shown that the manufactured chip is fully operational."