Experiment 5
The BJT in the Common-Emitter and Common-Collector Configurations

Introduction

The purpose of this experiment is to explore the behavior of the bipolar junction transistor (BJT) in the common-emitter (CE) and common-collector (CC) configurations. The loop containing the emitter junction is still considered the "controlling" loop; the loop containing the collector junction is considered the "controlled" loop. However, any of the three transistor terminals could be common to both the controlling and controlled loops. Each of these three possible configurations gives a different set of properties. The common-base (CB) configuration was explored previously; this experiment will compare and contrast the CE and CC arrangements.

Equipment Needed

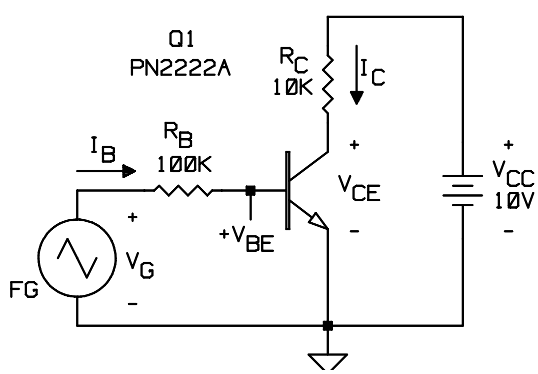
- Digital Storage Oscilloscope (DSO)
- Function Generator (FG)
- PN2222A npn Bipolar Junction Transistor (BJT)
- Lab Power Supply

Procedure

Connect the CE circuit of Fig. 1. Note that the emitter is common to the controlling and controlled loops. The scope ground clips, and the FG output cable shield can each be connected to the emitter separately by clipping them to short jumper wires inserted in the Protoboard.

1. Set the FG for a 2-Vpp 100-Hz triangle wave with a +1 V offset.

2. Observe both the circuit input voltage v_G and the circuit output voltage v_{CE} using the two-channel DSO in its voltage *vs.* time (Y-T) mode. The v_{CE} waveform should show evidence of operation in the cutoff, active and saturation modes at various points in the



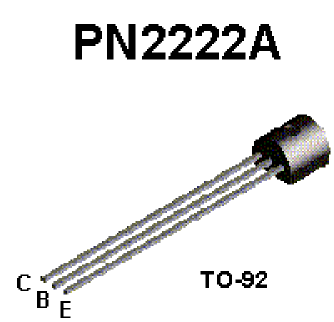


Fig. 1. Common-emitter circuit.

waveform. If it does not, adjust the FG amplitude to clearly show all three modes of operation of the BJT. Record the resulting pair of waveforms.

3. Place both baselines on center screen, and switch to the X-Y mode to obtain a plot of v_{CE} *vs.* v_G , with the origin at center screen. Record this plot, which should again have three distinct regions corresponding to three different modes of operation of the BJT.

4. Reduce the resistor R_B to about 50 K (you could either parallel an additional 100 K resistor, or substitute a 47 K resistor for R_B). Record Y-T and X-Y plots which show the effect this change has on the transfer behavior of this circuit.

5. Switch the DSO back to its Y-T mode. Set the FG for an output of 20-Vpp with zero offset. The collector-emitter voltage v_{CE} should be nearly a square wave. Record the v_G and v_{CE} waveforms on appropriate scales. This demonstrates a simple method of generating a square wave which is synchronized with the zero crossings of some other reference waveform.

Connect the CC circuit shown in Fig. 2. The input (controlling) loop includes the base terminal, as while as circuit ground. The output (controlled) loop includes the emitter terminal and circuit ground. Note that the collector is operated with a fixed (+5 V) voltage - this is considered the same as directly grounding the collector. In fact, the ground point between the two 5-V supplies could be moved to the top or the bottom of the two supplies, and the circuit would still be considered CC in any case.

1. Set the FG for a 20-Vpp 100-Hz triangle wave with zero offset.

2. Observe both the circuit input voltage v_G and the circuit output voltage v_E using the two-channel DSO in its voltage *vs.* time (Y-T) mode. The v_E waveform should show evidence of operation in the cutoff, active and saturation modes at various points in the waveform. Record these two waveforms.

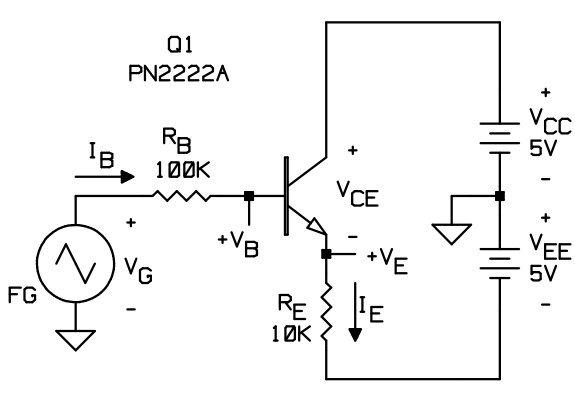


Fig. 2. Common-collector circuit.

3. Switch the DSO to its X-Y mode, and record v_E *vs.* v_G .

4. Use the DSO in both the Y-T and X-Y modes to document what happens when R_B is changed from 100 K to about 50 K.

Report

Write this report making reference to Experiment 4, the CB circuit. The CB circuit previously considered is probably the simplest to understand. You should have concluded from the text and the experiment that the collector loop current is controlled by the emitter loop current when the transistor is in the active mode, while both currents go to zero in the cutoff mode. These currents become solely dependent upon their own respective loop voltages and resistances in the saturation mode. In the active mode, the ratio of the collector current to the emitter current is approximately constant at the value "α," which is a transistor parameter. The input-loop (emitter) current is determined by a circuit including a voltage source, series resistance and a forward-biased pn junction. The output-loop (collector) current is approximately equal to the input-loop current. However, because the power supply voltage and resistance in the collector loop can be substantially greater than those in the emitter loop, the output-loop voltage can be an amplified replica of that in the input loop.

In writing this report, look for parallel observations in the CE and CC circuits.

1. In the CE circuit, quantitatively compare the input-loop (base) and output-loop (collector) currents.

2. In the CE circuit, describe what determines the input-loop current. What happens when the base resistor R_B is changed in value, all other things equal?

3. In the CE circuit, discuss the possibility of significant current gain (meaning that a small change in input current causes a large change in output current). Discuss the possibility of significant voltage gain (meaning that a small change in input voltage causes a large change in output voltage).

4. Interpret Fig. 1 as a crude analog-to-digital converter for the case of a large-amplitude input waveform. (Hint: The output waveform has essentially only two possible voltage levels: assign to one of them the binary digit "0," and to the other "1". What would knowing whether the output was "0" or "1" tell you about the input voltage?)

5. In the CC circuit, quantitatively compare the input-loop (base) and output-loop (emitter) currents.

6. In the CC circuit, did the value of the base resistor R_B have a strong effect on the input current, all other things being equal?

7. In the CC circuit, discuss the possibility of significant current gain (meaning that a small change in input current causes a large change in output current). Discuss the possibility

of significant voltage gain (meaning that a small change in input voltage causes a large change in output voltage).

8. Make a summary comparison among the three circuits studied thus far: the CB, the CE and the CC. Compare them in terms of their possible current gains (output-loop current *vs.* input-loop current), and their possible voltage gains (output voltage *vs.* input voltage).

<u>Sample Waveforms</u>

The waveforms below are samples obtained in developing this lab which are provided to illustrate what is to be expected. Do not use these in your report. The top two are from procedure steps 2 and 3 for the CE circuit. The lower one is from procedure step 2 for the CC circuit.