

Experiment 6 SPICE Modeling of the JFET and MOSFET

Introduction

The purpose of this experiment is to measure the parameters needed to model a JFET and a discrete MOSFET using SPICE. Only the dc characteristics are considered, and this is done using the simplest models available. The measured behaviors of several experimental circuits are compared with manual calculations and SPICE calculations.

Pre-Lab

The Appendix contains equations written in terms of the parameter names that SPICE is expecting to find on its .MODEL statements. Look up the corresponding equations in your electronics text and match these SPICE parameter names with those of your text. Find out how the traditional JFET parameters " I_{DSS} " and " V_P " relate to those of equations (1) and (2). Note that "WIDTH" and "LENGTH" refer to the physical dimensions of MOSFET: because the width and length of the discrete devices to be used in the lab are not known, these parameters will be set to equal values, thus canceling each other in the equations.

Equipment Needed

- Normal laboratory equipment
- 2N7000 n-channel enhancement-type MOSFET
- 2N5457 n-channel JFET (or 2N5458 - 2N5459)

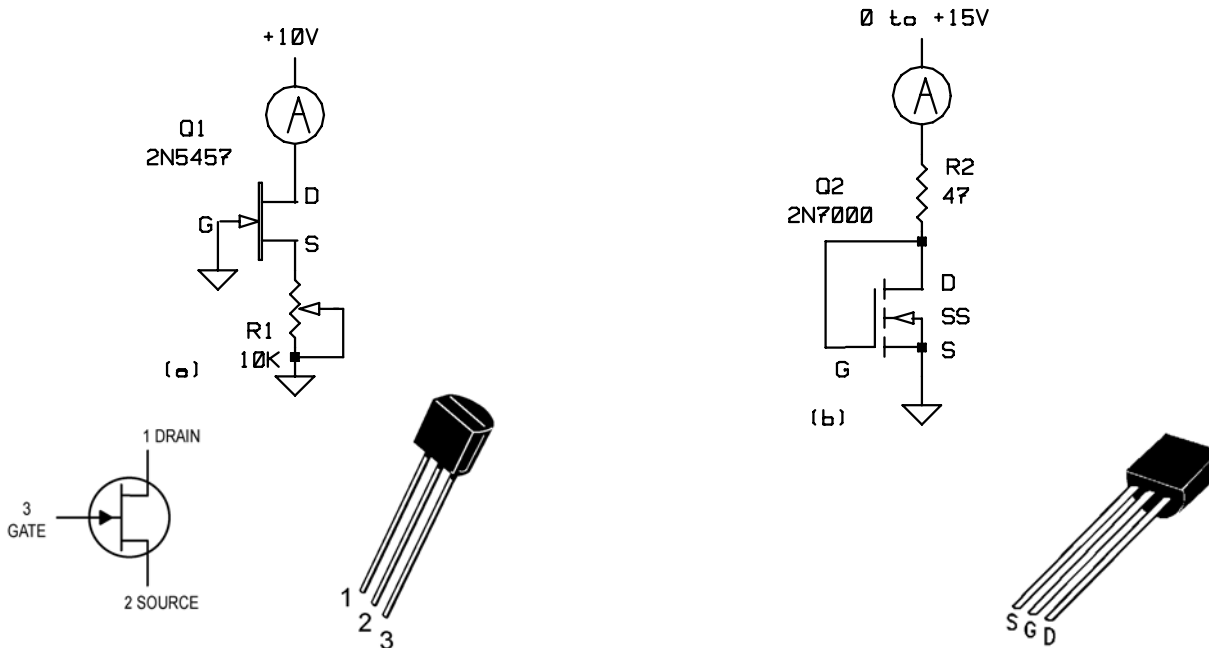


Fig. 1. (a) JFET test circuit. (b) enhancement MOSFET test circuit.

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Procedure

Fig. 1 shows test circuits for measuring key parameters of the JFET and MOSFET. Both of these circuits are designed to ensure constant-current mode (saturation mode) operation at all times. In both test circuits, the drain current (i_D) and gate-source voltage (v_{GS}) at four or more well-spaced data points are to be recorded. The data taken in the following procedure will later be processed to find the SPICE model parameters *for your specific part*, as opposed to data for a "typical" part.

1. Set up the JFET test circuit of Fig. 1(a). The ammeter will need to read drain currents up to about 20 mA. Use a DVM to record the gate-source voltage v_{GS} .
2. Short the source directly to ground ($v_{GS}=0$) and record i_D . Note that there will be some drift in the measured value as the JFET warms up - try to record a cold value. This test gives the value of " I_{DSS} ".
3. Adjust the potentiometer R1 for several values of i_D ranging from nearly I_{DSS} to less than one-tenth of that value. Record three more well-spaced $i_D - v_{GS}$ data pairs.
4. Set up the MOSFET test circuit of Fig. 1(b). The ammeter will need to read drain currents up to about 100 mA (the 2N7000 is a higher-current device than the 2N5457). Use a DVM to record v_{GS} .
5. Vary the supply voltage as needed to obtain drain currents ranging from 1 mA to 100 mA. Record four well-spaced $i_D - v_{GS}$ data pairs over this range.

Set up each of the circuits in Figs. 2 and 3. Record the $i_D - v_{GS}$ pairs in obtained in each case. Keep the specific two transistors used by your laboratory group in a safe place until the report for this lab is successfully written. Should you find that there would be any question about the validity of the data you have taken, you could re-check your data points.

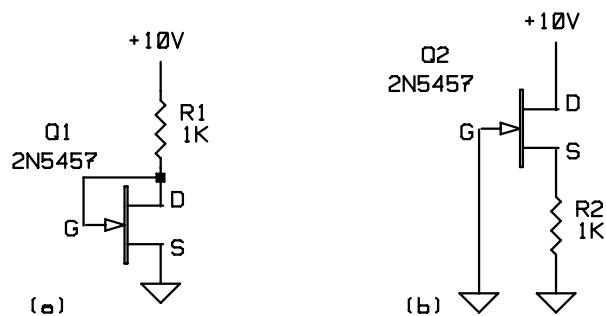


Fig. 2. JFET circuits.

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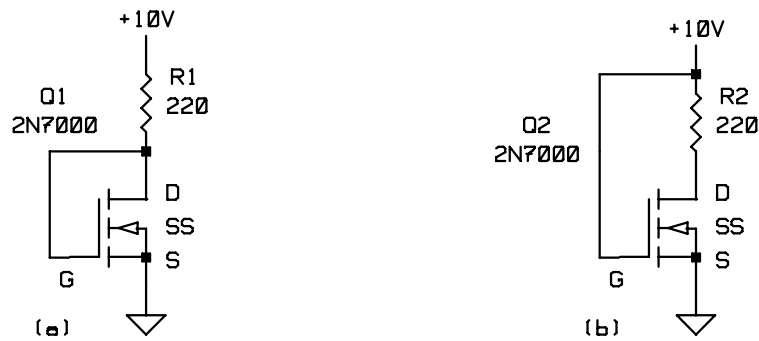


Fig. 3. MOSFET circuits.

Report

The report has three main themes: (1) the interpretation of the data taken using Fig. 1 to find model parameters for the FETs, (2) hand computation of the expected $i_D - v_{GS}$ solutions for the circuits of Figs. 2 and 3, and the use of SPICE together with your measured model parameters to compute solutions for the circuits of Figs. 2 and 3. You should also examine the data sheets for the devices used in this experiment, and *using only the information found on the data sheets* make the best possible estimation of the solutions for Figs. 2 and 3. Your report should include the following points:

1. How do you know that the FET can only operate in its constant-current region in the circuits of Fig. 1?
2. Use the procedure illustrated in Fig. 4 of the Appendix to derive V_{TO} and BETA or KP from the data taken using Fig. 1. Discuss the procedure.
3. Use the measured values of V_{TO} , BETA and KP to hand calculate i_D and v_{GS} in Figs. 2 and 3. Relate these parameter names to the ones used in your electronics text.
4. Use SPICE to run a DC analysis based on your measured parameter values. Include the SPICE output file with your results in an appendix to this lab report. Compare these results with your hand-computed solutions.
5. Use the SPICE models for a "typical" device to solve the circuits of Figs. 2 and 3. Compare with your lab results.

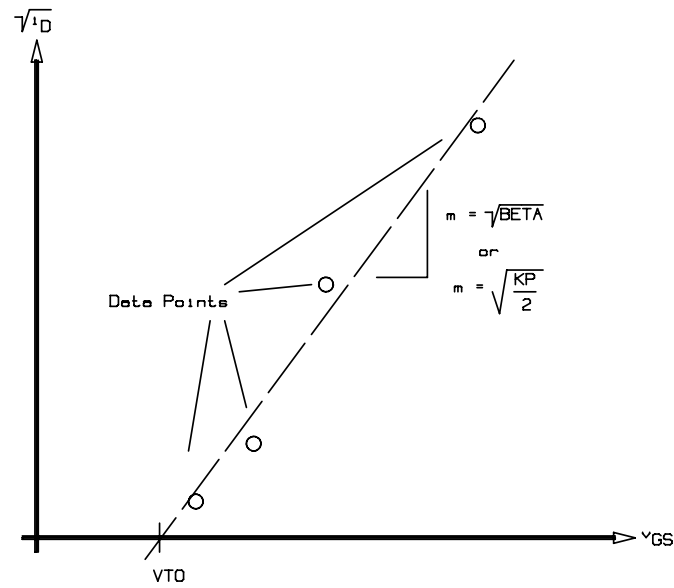


Fig. 4. Best-fit plot of square-root of i_D vs. v_{GS} .

Appendix

The SPICE JFET model¹ assumes that whenever v_{GS} is above its threshold (pinchoff) value, the JFET behaves according to the following dc equations:

$$i_D = BETA [v_{GS} - VTO]^2 \quad \text{for} \quad v_{GD} \leq VTO \quad (1)$$

$$i_D = BETA [2(v_{GS} - VTO)v_{DS} - v_{DS}^2] \quad \text{for} \quad v_{GD} \geq VTO \quad (2)$$

The SPICE level 1 MOSFET model assumes that whenever v_{GS} is above its threshold value, the MOSFET has the following dc behavior:

$$i_D = \frac{WIDTH}{LENGTH} \frac{KP}{2} [v_{GS} - VTO]^2 \quad \text{for} \quad v_{GD} \leq VTO \quad (3)$$

$$i_D = \frac{WIDTH}{LENGTH} \frac{KP}{2} [2(v_{GS} - VTO)v_{DS} - v_{DS}^2] \quad \text{for} \quad v_{GD} \geq VTO \quad (4)$$

The experimental $\sqrt{i_D}$ vs. v_{GS} data are plotted as shown in Fig. 4. The best-fit line drawn through the data points determines VTO (the v_{GS} -axis intercept) and $BETA$ or $KP/2$ (the square of the slope of the line). This can be derived from (1) or (3).

¹ The channel-length modulation parameter "LAMBDA" is being taken equal to zero for both JFETs and MOSFETs.