

Experiment 7

Characterizing Digital Logic Gates

Introduction

The purpose of this experiment is to measure the speed of two families of widely-used digital logic gates. 4000-series CMOS is a slow aluminum-gate technology which has excellent noise margin and a supply voltage range of 3 to 15 V. 74LS00-series TTL is a faster bipolar logic family which is designed for a 5 V (+- 5%) supply voltage.

Equipment Needed

- Normal laboratory equipment
- '4011 CMOS quad NAND gate
- '74LS00 TTL quad NAND gate

Procedure

Connect the circuit of Fig. 3 using the CMOS logic gate (MC14011 or CD4011). Consult Fig. 1 for the correct pin numbers. Note that the 3-foot coaxial cable from the function generator to the circuit is shown explicitly: this cable is a 50- Ω transmission line. R1 (56 Ω) is included in the circuit to improve the termination of this cable and reduce the reflection of the steps in the FG output voltage¹. Set the power supply for 5 V (4.95 - 5.05 V). Bypass capacitor C1 must be connected directly between pin 7 (GND or V_{SS}) and pin 14 (V_{CC} or V_{DD}) of the integrated circuit package. Connect channels 1 and 2 of the scope to the locations indicated. The capacitors C_p represent the scope probe capacitances. For the HP 54600, C_p is 16 pF.

1. Set the FG for a square-wave output at 1 MHz, 5 V_{p-p}, 2.5 V offset. You may leave the FG in its power-on default condition in which it assumes you have given it a 50- Ω termination (which is the case). Use Ch. 1 of the scope to verify that the logic gate is getting an input voltage which transitions between 0 and 5 volts.
2. Ch. 2 should show a gate output signal which is logically inverted with respect to Ch. 1. Measure the rise times (t_R)² of the input and output signals. Measure the propagation delay³ for the low-to-high output transition (t_{PLH}), and for the high-to-low output transition (t_{PHL}). The scope can automate these measurements using selections under "Measure Time." You may need to set the trigger for rising or falling edge, and set a menu selection of which input and output transition is to be detected by the measurement. Record the scope screen showing the input and output signals at the gate, with the output low-to-high transition in the center of the screen at 50 ns/div.

¹ The propagation speed of the transmission line is about two-thirds the speed of light, or roughly 2/3 feet/ns. For a 3-foot line, this implies a 4.5-ns delay for a one-way trip, or reflections (anomalies) in the pulse waveform at Ch. 1 spaced at about 9-ns intervals.

² Rise time is the time needed for a step signal to go from 10% of its ultimate step change to 90% of its ultimate step change.

³ Propagation delay is the time elapsing from the midpoint of the input step transition to the midpoint of the output transition.

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3. Raise the power supply voltage to 10 V and remove R1 to double the voltage delivered to the gate input. (This may also degrade the waveshape somewhat by causing ripples (reflections) to appear immediately after the steps.) Measure t_{PLH} and t_{PHL} again. Record the gate input and output signals for an output low-to-high transition again at 50 ns/div. Add an additional 33 pF of load capacitance and record the resulting change in t_{PLH} .
4. Re-connect Fig. 3 using the TTL logic gate ('74LS00). Consult Fig. 2 for the correct pin numbers: the CMOS and TTL devices have different pin-outs. Be sure to reset the power supply to 5 V, and replace R1 in the circuit. Measure t_r of the input and output waveforms. Measure t_{PLH} and t_{PHL} . The propagation delays for the LS-TTL device should be measured at the 1.3-V crossings, not the mid-crossings of the input and output waveforms. You may do this semi-automatically by using the cursors to get time readouts at these points.
5. Fig. 4 gives a quick way to estimate the average propagation delay for an odd number of gates (3 in this case). Connect Fig. 4 using the CMOS gate ('4011) and a 5-V supply. It should self oscillate with a quasi-pulse waveform: measure the period of the oscillation. Record the period for supply voltages of 5 V, 10 V, and 15 V. Record a sample waveform for any one of these cases.
6. Connect Fig. 4 using the TTL gate ('74LS00) and a 5-V supply. Record the period of the self oscillation.

Report

1. Show the propagation delay waveforms recorded in step 2. Mark these waveforms to show where the propagation delay was measured. Explain as needed.
2. Show the propagation delay waveforms recorded in step 3. Discuss the effects of raising the power supply voltage, or increasing the load capacitance, on the speed of the 4000-series CMOS logic family.
3. Use the data generated in step 4 to compare the speeds of LS-TTL and CMOS. Determine why the propagation delays in LS-TTL are measured at the 1.3-V crossings instead of the waveform midpoints. (Hint: Get a data sheet and look up the maximum valid input-low voltage, and minimum valid input-high voltage for LS-TTL.) Are TTL propagation delays the same for both the low-to-high and high-to-low output transitions?
4. Use the ring oscillator data to estimate the average propagation delays for CMOS at 5, 10, and 15 volts, and for LS-TTL. The estimation formula is:

$$t_{PROP} = \frac{Period}{2N} \text{ where } N = 3 \text{ gates}$$

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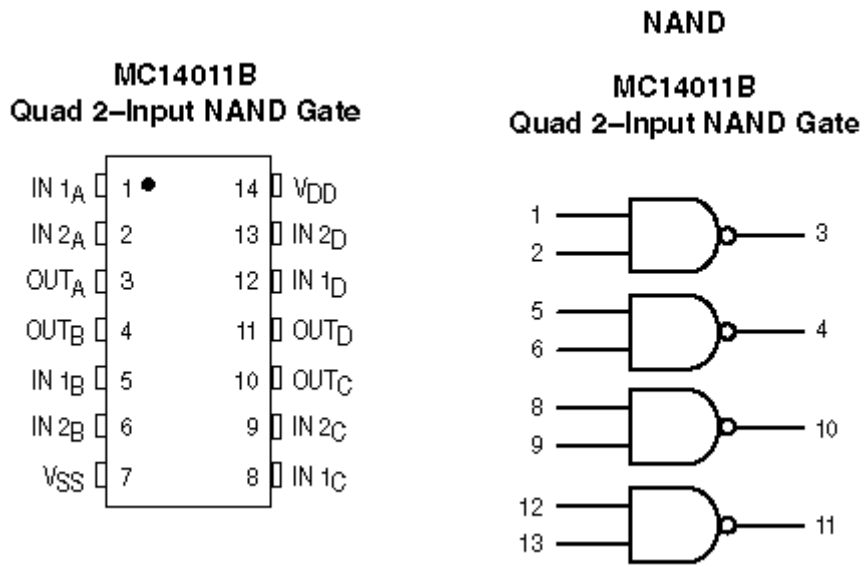


Fig. 1 Top view and pin-outs for MC14011 (CD4011) quad-NAND gate.

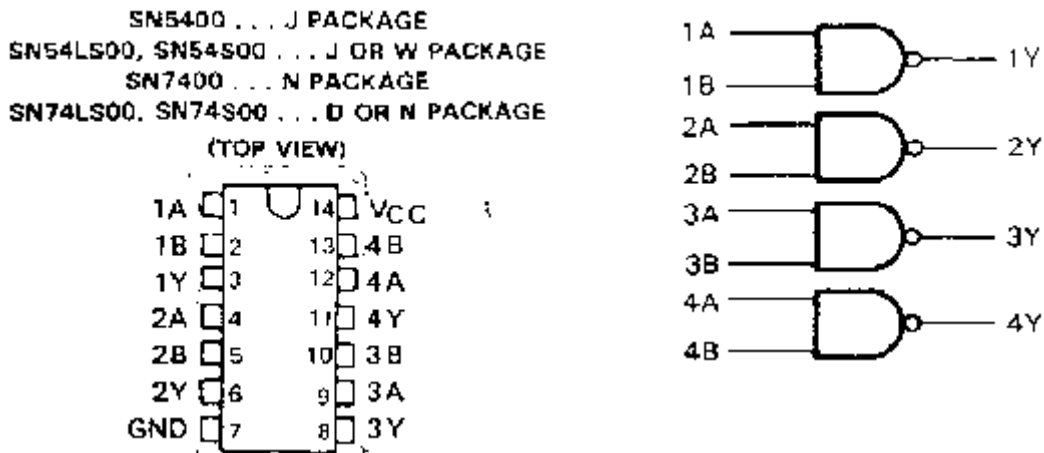


Fig. 2 Top view and pin-outs for SN74LS00 quad-NAND gate.

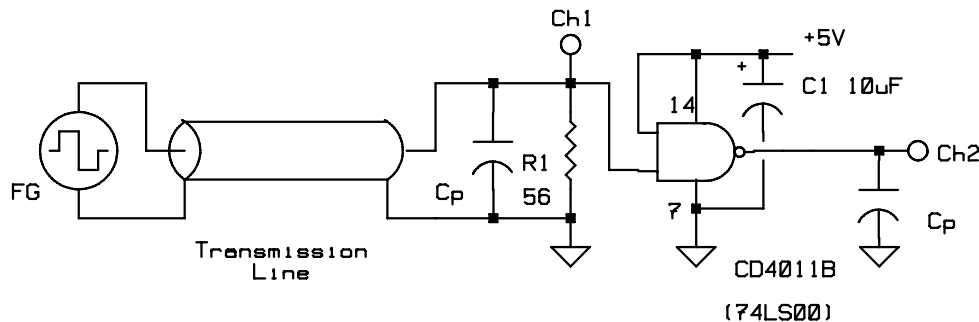


Fig. 3 Measuring propagation delay and rise/fall times. C_p is the scope probe capacitance.

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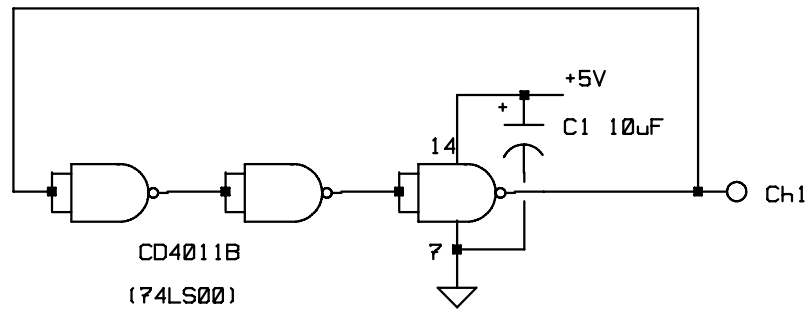


Fig. 4 Ring oscillator for measuring average propagation delay.