Lab Project 3:

In projects 1 and 2 you developed software that tests memory location to ensure that data can be written to and read from them properly. This software was created for a couple of reasons. One is to help you, the student, better understand the Assembly language and how the processor works internally in addition to externally with memory. A second reason for its creation is that it will be used to help test the hardware you design and implement in projects 3 and 4.

Projects 3 and 4 emphasize the development of circuitry for interfacing the CPU with memory. Project 3 will begin with the design of the buffering and demultiplexing circuitry. This circuitry will be tested by hardwiring an instruction to the bus and verifying the instruction with the Chameleon software and a logic analyzer. Project 4 will finish the design by implementing the remaining control signals, connecting the data and address bus to the RAM and ROM, and further implementing the control signals.

Goals:

- To design and prototype the required minimum buffering and demultiplexing circuitry for the 80186XL CPU.
- Use the logical analyzer and in-circuit emulator for debugging and system integration purposes.

Requirements:

- Design and implement the buffering and demultiplexing circuitry for Intel 80186XL CPU.
- Hardware the instruction \texttt{HERE: jmp HERE} to the data bus.
- The hardwired instruction should be executed upon CPU reset only.
- For logic high use a 5 volt supply through a 1K-Ohm resister.
- When designing the board, take into account the future work required for project 4. Board real-estate should be use conservatively. The circuitry for the hardwire instruction and address detection will be removed for project 4; however, the latching and buffering hardware will remain in place.
- Ensure that input pins to the processor are not floating. Tie them to either high or low.
- Design a test procedure to ensure that the address is latched, and the instruction appears on the data bus. The in-circuit emulator and logical analyzer should be used. For the in-circuit emulator, ensure that the address for the instruction is mapped to USR and not ICE.
- Your lab TA will demonstrate how to use the prototype boards and will distribute the needed materials and tools for the project. Keep these tools for the forth project.

Deliverables:

- Demonstrate your circuitry to your lab instructor.
- Turn in a professional quality report. Formatting should coincide with the document on report formats. Correct spelling, grammar, and coherence as well as
level of professionalism should be used in your report as these will be factors in grading.

- Indicate team member contributions.

Questions
1. What other ways could be used to implement the address detection?
2. Are these other schemes more or less efficient? If so in what way? (Cost, efficiency, implementation time, etc).
3. If no address detection was used, what would be the result? Would this have any affect on the actual execution of the processor?